LLRF Upgrade Results and Plans for Run 10, L-10 Cavity Upgrade

RHIC Retreat '09
K. Smith, 07/16/2009

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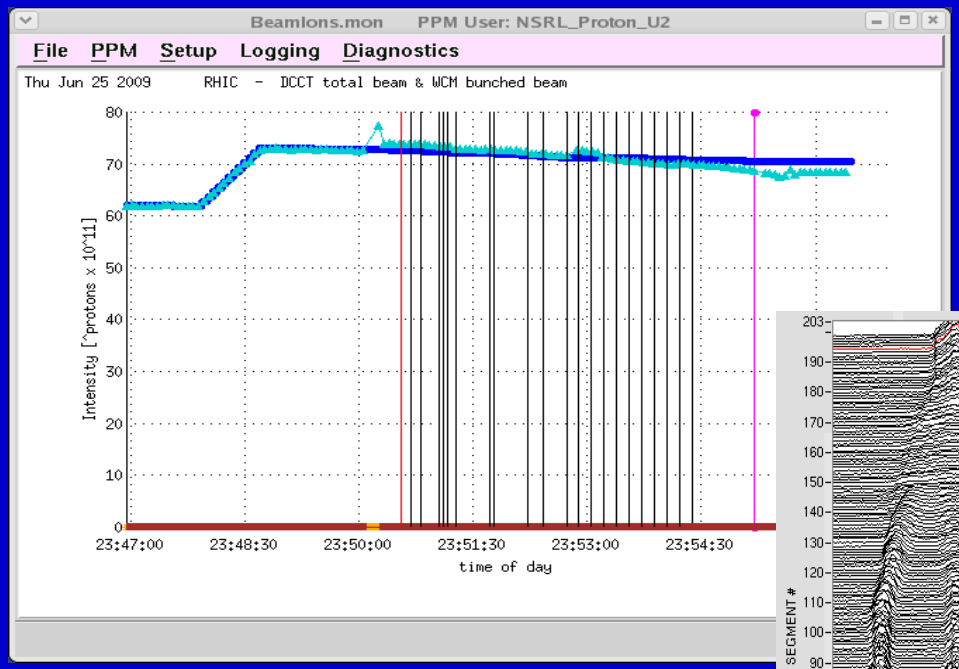
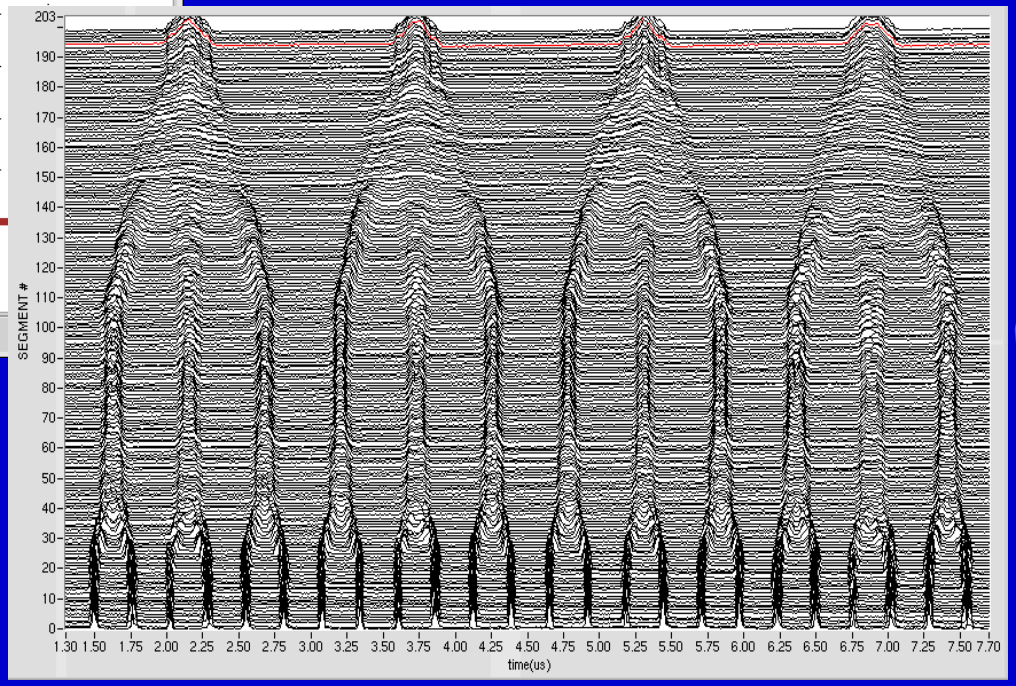
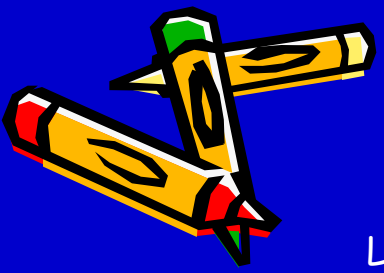
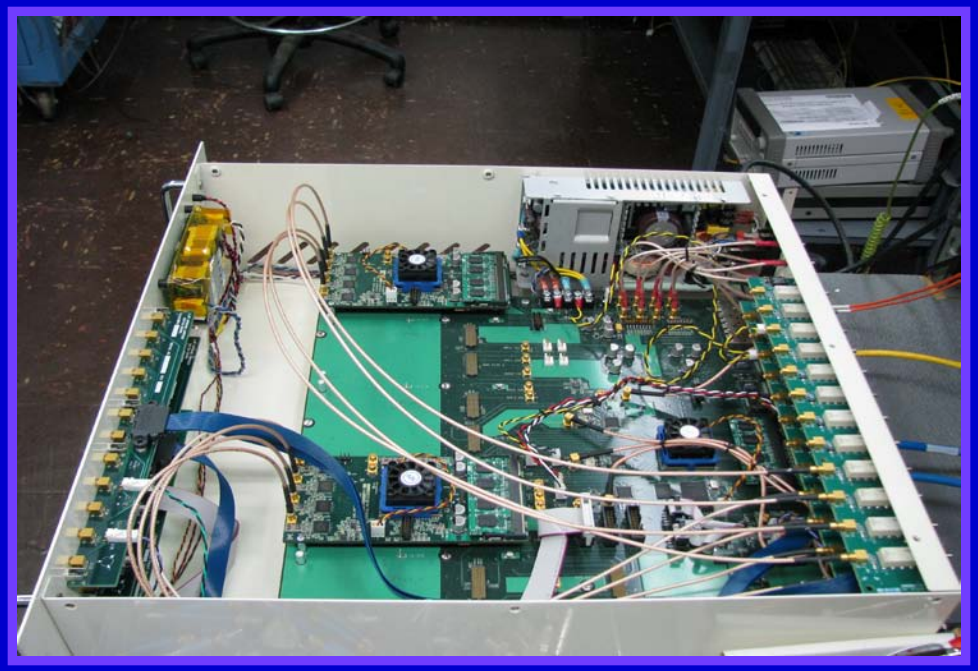






Refresher: Goal of the LLRF Upgrade

- Design a stand alone, generic, modular digital controller architecture which can be configured to satisfy all of the LLRF control demands we currently have, and which will be supportable and upgradeable into the foreseeable future. It has potential applicability to many tasks …



- LLRF "Controller" (Appendix A)

- Integrate seamlessly into existing controls infrastructure, be easy to deploy, provide access to all relevant control parameters (eliminate knobs), provide vastly improved diagnostic data capabilities, and permit remote reconfiguration.
- The "why" has been discussed in prior presentations.

- Original "LLRF Upgrade" scope was simply to replace the RHIC cfe-4a-rfb2 and cfe-4a-rfy2 VME crates. So we'll finally be there come Run 10.

Results From FY '09 Efforts

- Two days of about 10 hours each were used to perform first commissioning of LLRF Upgrade systems at RHIC.
- System development efforts continued unabated before, during and after these commissioning efforts.
- Hardware, firmware and software configurations were changing in real time to address issues as they were encountered.

- Day 1: April, using the 250 GeV PP machine just prior to the 100 GeV PP switchover.
  - Goal:
    - Demonstrate injection and injection cogging in the Blue ring.
    - Doesn't sound like much, but it was in fact a huge milestone for the overall effort.
  - Achievements:
    - First real test of a fully integrated system operating in its native habitat – the machine.
    - Two operational embedded FECs, integrated seamlessly into the controls network.
    - Embedded Event Link and RTDL decoders, and V202 functionality operational in hardware.
    - 2.5 Gbit/s "Aurora" serial links providing carrier to daughter, carrier to carrier communication.
    - 1 Gbit/s serial "Update Link" providing synchronous data and timing information across entire system.
    - RF synthesizers implemented and synchronized across multiple RF DAC daughter modules.
    - "Program" and "Feedback" DSPs implemented on RF DAC daughter modules.
    - Remote (network) reconfiguration of all hardware tested, and in fact used out of necessity.
    - Tested all necessary ADOs, PET pages, software apps (e.g. RHIC Injection), etc.
    - And as an aside, demonstrated injection, injection cogging and open loop acceleration to store.
  - Payoff:
    - First commissioning day allowed us to learn a great deal about the integrated system, to correct or at least gain the insight needed to correct observed problems, and put us in a great position to achieve the next milestone.

Results From FY '09 Efforts

- Day 2: June, using the 100 GeV machine prior to end of PP run.
  - Goal:
    - Demonstrate acceleration to flat top with LLRF feedback loops active.
    - Demonstrate same for yellow, synchro machines, cog to collision, walk away.
  - Achievements:
    - Successfully accelerated ~75 bunches (in a 98 bunch pattern) to flat top, LLRF feedback loops closed, with good efficiency.
    - First test of new bunch to bucket (btb) phase detector and first test of Feedback DSP operating in various loop modes.
    - Again, easier said than done.
      - BTB Phase Detector
        - » RF ADC daughter module with firmware designed to obtain bunch by bunch phase info for up to a 120 bunch pattern, provide average phase error for btb phase loop, injection phase error data for injection tuning …
        - » Worked. Showed some pathological behavior which we must correct prior to FY '10 start-up.
      - Feedback DSP
        - » The brains of the LLRF control loops. Manages loop states, implements feedback algorithms, primary source of system diagnostic data …
        - » Worked nearly flawlessly. Couple of incorrect variable pointers and such. All observed problems have already been corrected.
    - Did not test Yellow side due to time constraints. Did not leave system operational.
  - Payoff:
    - Believe we've gained sufficient knowledge and understanding of observed issues to be confident about an FY '10 start-up with the new LLRF in place.
    - Plenty of work to be done between now and then.

The Plan For Run 10

- RHIC LLRF
  - Start RHIC with new LLRF System ready to fully commission.
  - Integrate quad mode damping from the start.
    - One example of the flexibility of the new system.
    - "Readily expandable, flexible, obsolescence resistant, ready spares. Example: Once new system is stable, new quad mode damper functionality is readily subsumed and current "external" implementation goes away." (RHIC Retreat 2008)
  - Begin commissioning of "Cavity Controllers" during the Au run.
    - Provide independent drive for each cavity, eliminate existing IQ modulators.
    - In the fullness of time add tuning loop, phase and amplitude stabilization, monitoring …
  - This remains a commissioning effort and we will need machine time.
    - Blue Injection, Timing Setup, Injection Correction, Capture — 1 x 12 Hrs
      - Testing and debugging of BTB Phase Detector
    - Blue Acceleration, Transition Crossing, Store Cogging Testing, Rebucket Testing — 2 x 12 Hrs
      - Testing and debugging of BTB Phase Detector, Feedback DSP, DAC Firmware
    - Yellow Injection, Timing Setup, Injection Correction, Capture — 1 x 12 Hrs
      - Ditto Blue.
    - Yellow Acceleration, RTR Synchro, Transition Crossing — 1 x 12 Hrs
      - RTR Synchro loop moves from analog to digital
    - Collision Cogging, Rebucketing — 1 x 12 Hrs
      - Rebucket gymnastic is a new implementation, simpler in hardware.
    - Quad mode damping — 1 x 8 Hrs
      - Completely new implementation, embedded in new hardware (firmware)

- EBIS LLRF (Cavity Controllers)
  - Provide RF drive and tuning control for 5 systems.
- ERL LLRF (Cavity Controllers)
  - Provide phase locked RF drive for 5-cell and gun.

AGS L-10 Cavity Upgrade

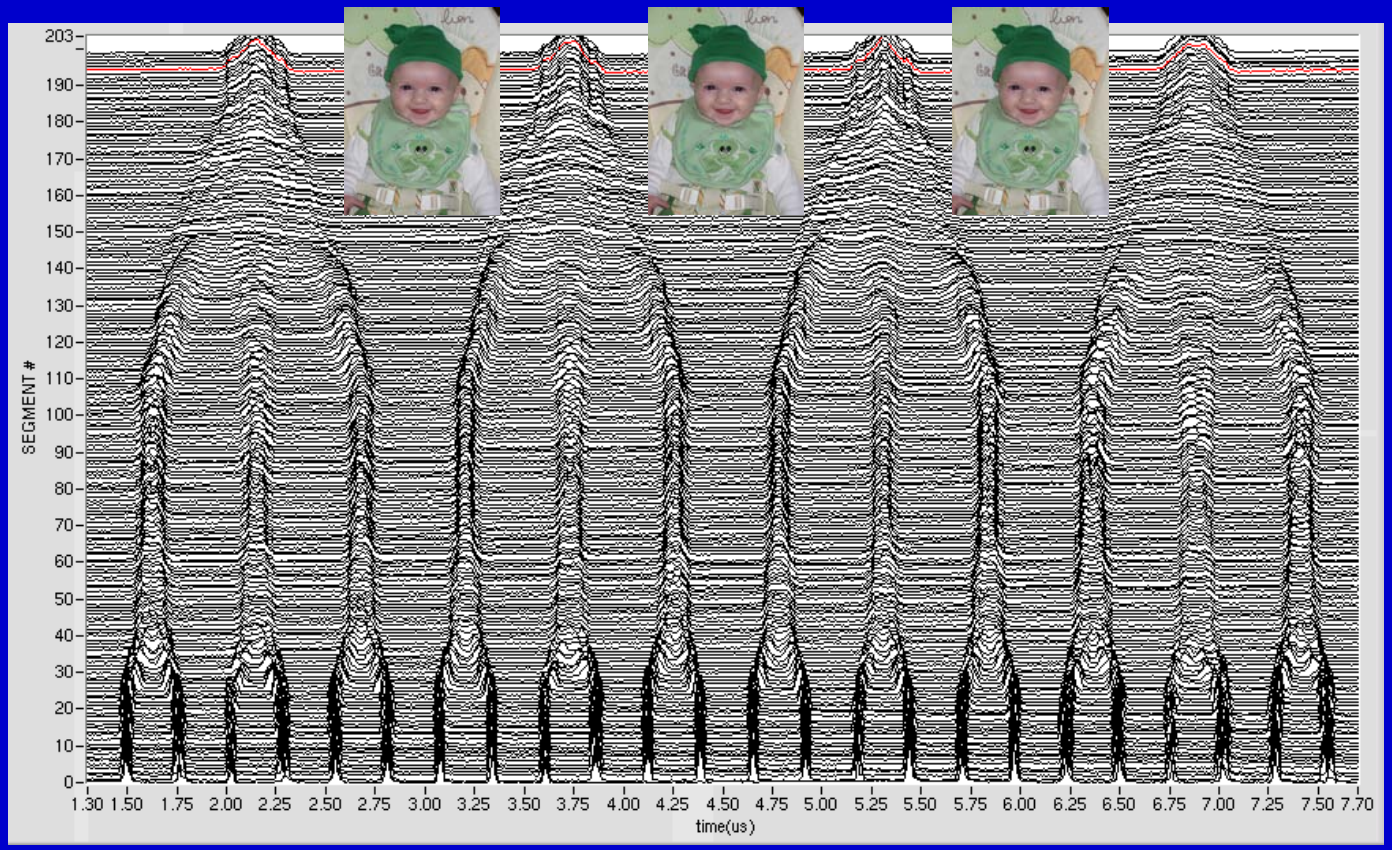
- What, why, how?
  - The "old" AGS L-10 cavity was a broadband cavity (finemet) originally installed to explore the use of barrier buckets to increase proton intensity.
  - Its application for RHIC heavy ions was in enabling the original debunch-rebunch scheme, and lately the 24=>12=>4 bunch merging scheme for increasing bunch intensity.
  - Cavity was "one off", difficult to maintain, of questionable reliability = single point failure waiting to happen (no spare).
  - Cavity ran h=4 and h=8 simultaneously as part of the gymnastic. This greatly enhanced the odds of inadvertently inducing a failure. In fact we did kill it at least once.
  - Performance was less than ideal, leading to excessive longitudinal emittance growth.
  - Solution was to modify an existing AGS spare cavity for operation at the required very low h=4 frequency, about 600 kHz.
  - Modify a second AGS acceleration cavity to run h=8, making h=4 and h=8 actually orthogonal.
  - Add feedback loops to improve phase and amplitude stability (low frequency is hard on the cavity ferrite), which will result in improved longitudinal emittance preservation during the merge gymnastic.
  - Will also improve reliability and serviceability via commonality with existing AGS acceleration cavities. Not quite identical, but very close. Certainly provides us with spare capability.

AGS L-10 Cavity Upgrade

- What is the merge?

4 Bunches Come Out (Usually)

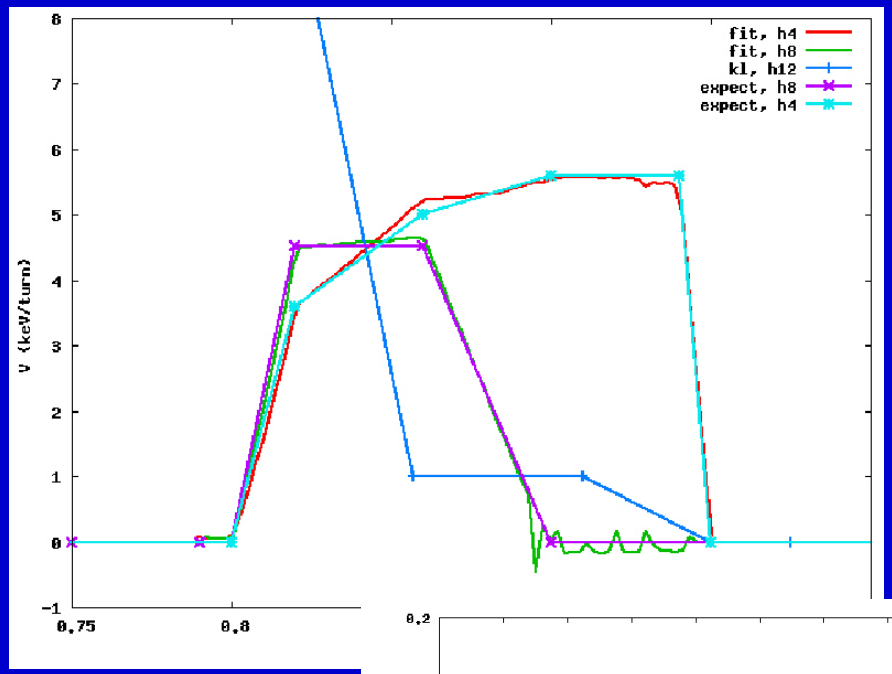
Time Into The merge Gymnastic ->



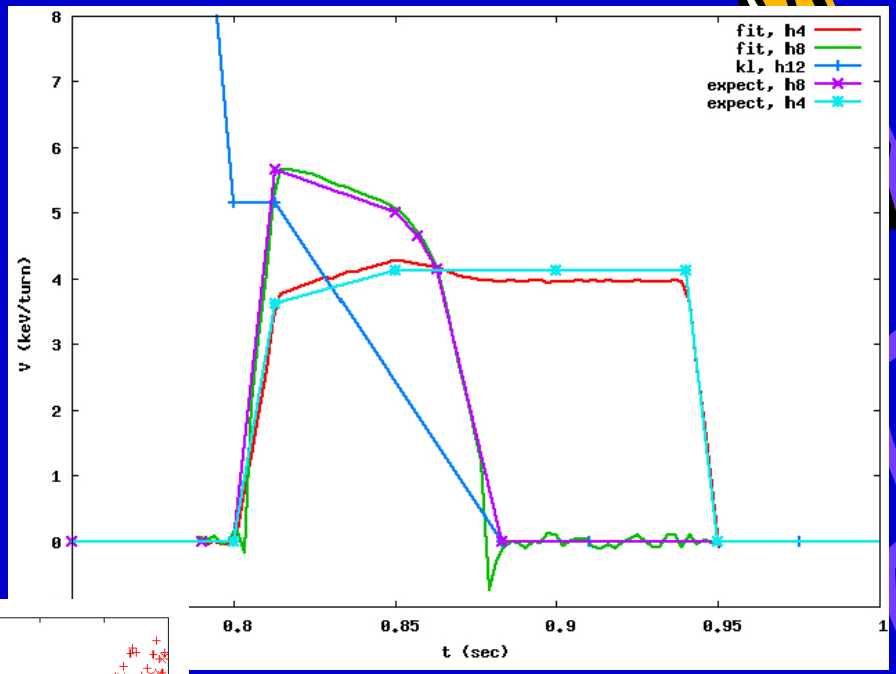
24 Bunches Come In
4 x 6 bunches per Booster transfer

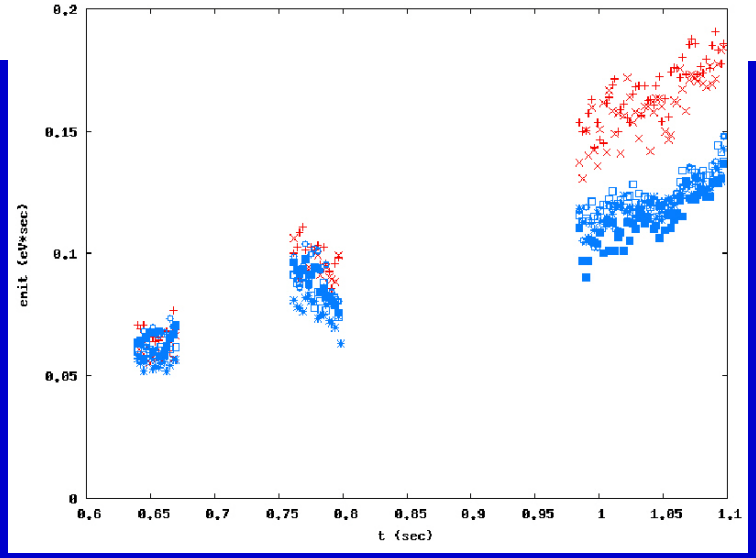
AGS L-10 Cavity Upgrade

Non-Optimal Program



Optimal Program



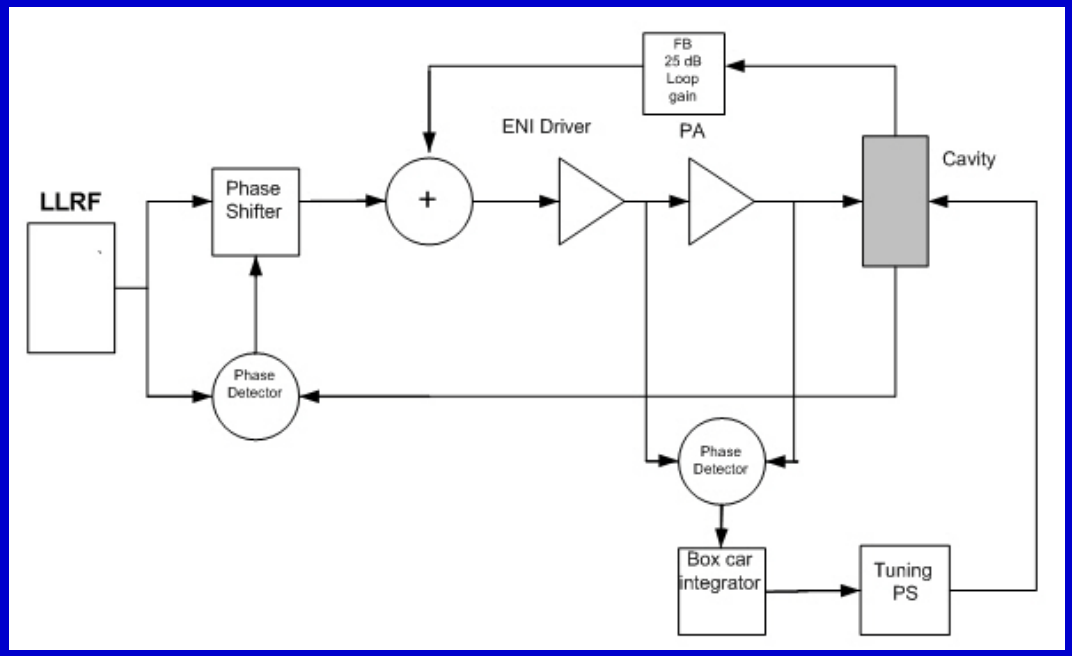


Red: Non-Optimal Merge

Blue: Optimal Merge

Emittance improvement via voltage program optimization.

AGS L-10 Cavity Upgrade



New L-10 RF System

- Cavity will run single harmonic, h=4.
  - Second AGS acceleration cavity modified for h=8. It remains a "standard" acceleration cavity, except for extra capacitive loading.
- Inner wideband RF feedback loop provides first order phase and amplitude stabilization.
- Tuning loop provides slow cavity resonance drift stabilization.
- Outer phase loop improves overall phase stabilization. Cavity tuning angle is a strong function of voltage.

The End

LLRF Would Like To Express Its Strong Support For A Call-In Free Holiday Specifically Honoring Single Parent "Moms" Of Any Gender In Unconventional Family Units

Appendix A: "Controllers" ???

- Primary LLRF Hardware Development Effort: The LLRF Controller
- A Controller is a configurable hardware platform, the basic building block from which a complete LLRF system is built.
  - "System Controller": Frequency program, beam control loops, synchro loops, damping, adaptive loops (cycle to cycle feedback), etc.
  - "Cavity Controller": Individual cavity amplitude, phase, tuning, control of other HLRF parameters.
- A Controller is configured as needed from two major components:
  - "Controller" = "Carrier Board" + N "Daughter Cards"
  - Both the Carrier and Daughter designs center on a common, powerful FPGA family, Xilinx Virtex-5.
  - Carrier Board
    - Stand alone control system interface. The C-AD Control System sees it as a standard FEC. Compatible with all Controls system infrastructure.
    - Daughter host platform, system power source, system status monitor, communication hub, data acquisition engine, update and controls link receiver.
  - Daughter Cards
    - Provide system specific functionality via data converters and processing horsepower.
    - All daughter modules reuse a common "back end" digital architecture providing the carrier interface and support for all standard daughter features (e.g. DDR2 SO-DIMM, FLASH, Power Converters …)
    - ADC, DAC, FPGA, DSP …

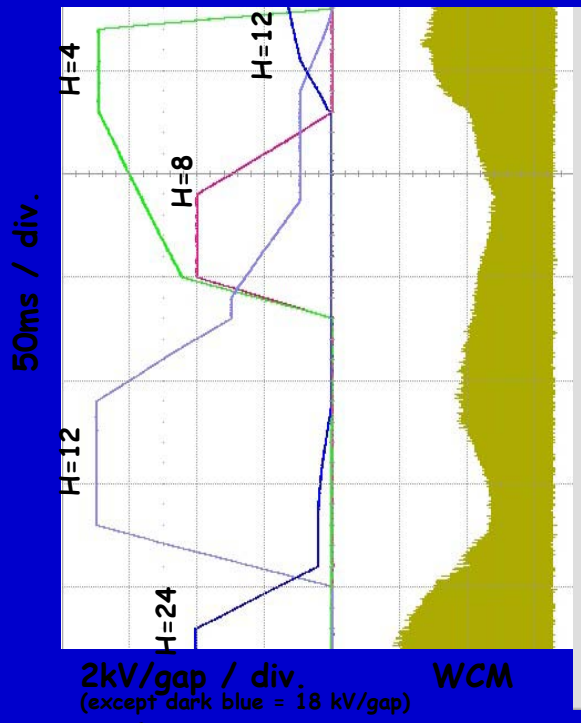
Appendix B: World's Shortest Dictionary

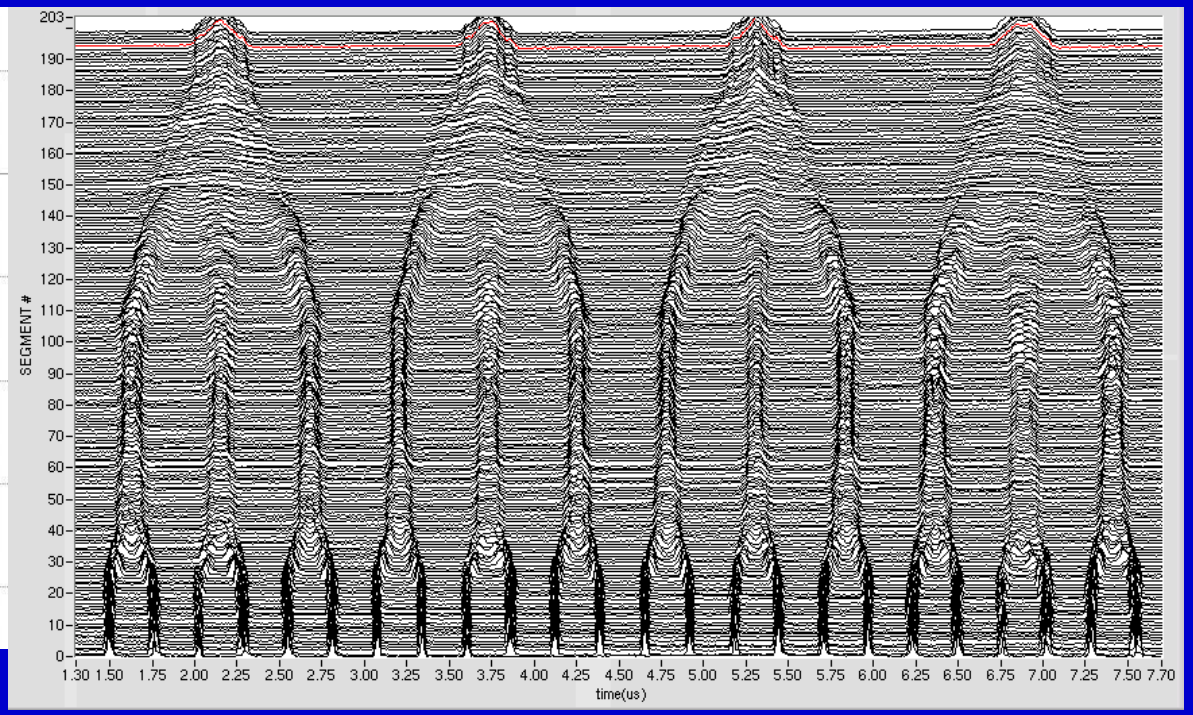
- Firmware vs. Software
  - Software is what most of you know as software: computer application programs, scripts, ADOs, etc.
  - Firmware refers to a specific type of program, written in a specialized language, used to describe the internal functions of our FPGAs. Ultimately it is implemented (synthesized, mapped, placed and routed) within the programmable fabric of the FPGA to provide the desired functionality. Thus "firmware", as it is software that becomes hardware.
  - FPGA = Field Programmable Gate Array. A "chip" containing a large array (the "fabric") of programmable logic elements, memory and often other specialized units (processors, serial transceivers, DSP units, etc.). It provides an enormously powerful and flexible platform for implementing all manner of digital systems.

Appendix C: 2007 Au Bunch Merge Time Meeting Presentation

A Sort of Graphical Representation

- For the Au07 run, we have reconfigured the AGS LLRF to accommodate a two step bunch merging scheme.
  - Step1: 2:1 Merge, 24 bunches to 12 bunches
  - Step2: 3:1 Merge, 12 bunches to 4 bunches

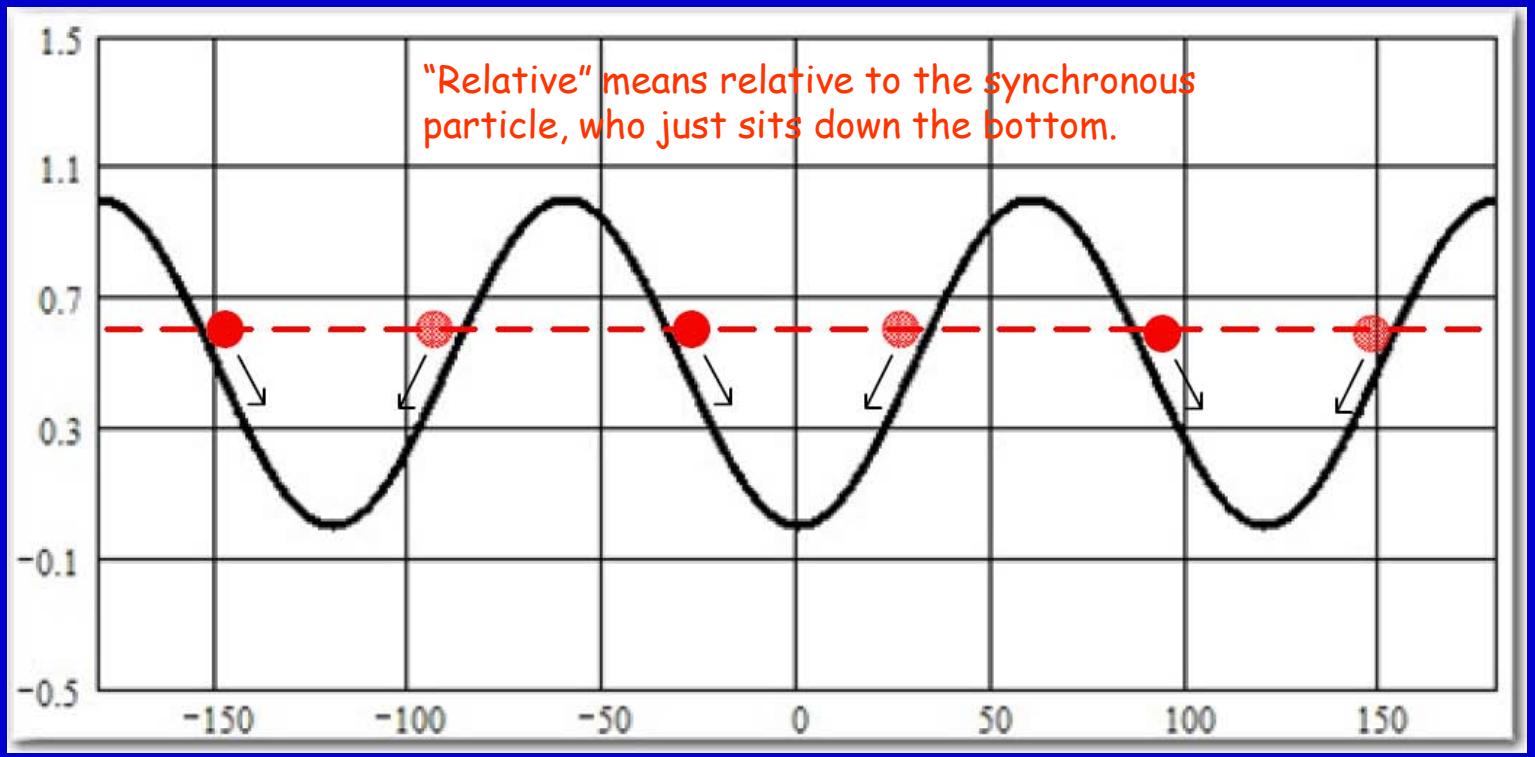




- "Mountain Range" Plot

A few details need to be explained …

An RF bucket is a potential well that traps particles with less than a certain maximum +/- *relative* energy error.



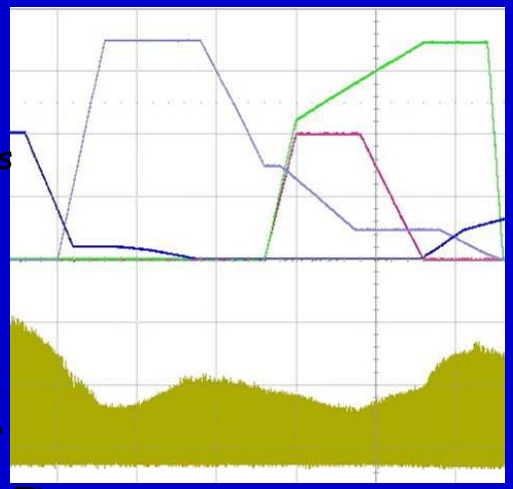
Some concepts to keep in mind:

1) A particle escapes the well when it has enough energy.
2) One way to describe a particle's location is by specifying its phase (or time) and its energy (phase space plots to come later).
3) Another way is to refer to its neighbourhood, the area within the well contained by the particle's trajectory (emittance, eV*s).
4) An adiabatic change means you don't change the particle's total energy, which means you don't change the size of its neighbourhood. You can however change the basic shape of the neighbourhood.

What we're gonna do in the merge is to use a combination of potential wells and vary them in time (adiabatically) to try and merge the two outer bunches with the center bunch. A bunch is just a big collection (say 10^9) of particles inhabiting the potential well.

RF Voltages

Wall Current Monitor



Time =>
50ms/div

^
We are here.

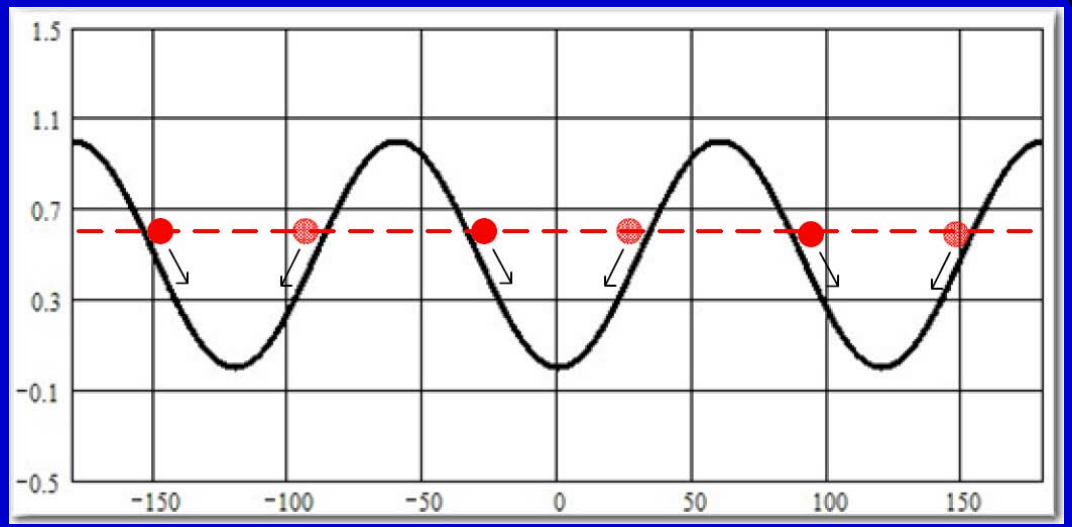
"h" means harmonic number, the number of buckets which that particular RF produces in the ring.

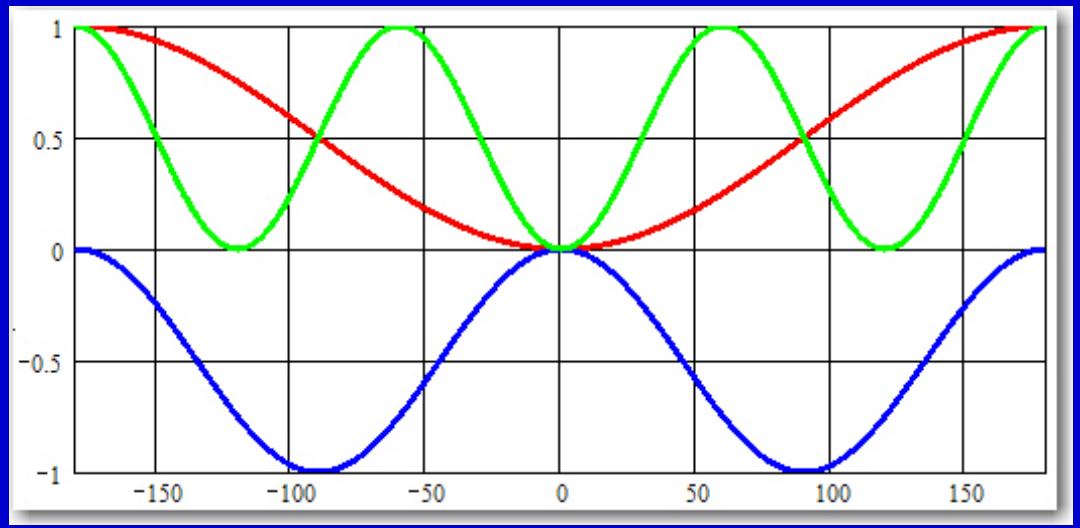
(RED) h = 4

(BLUE) h = 8

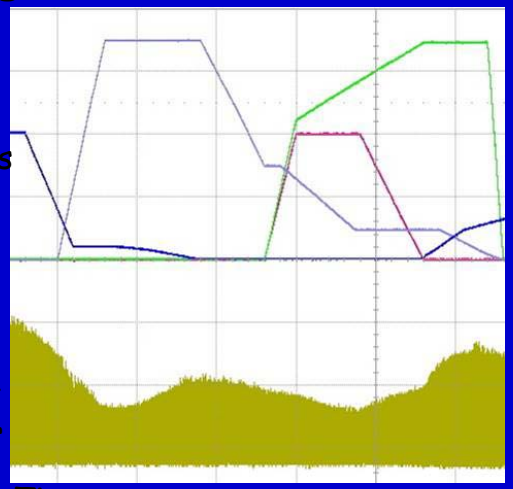
(GREEN) h = 12

We'd like to move from just the green guy, to just the red guy, with no real estate tax.





A nice merge is one that is adiabatic, and so does not increase the total size of the neighbourhood inhabited by the bunches being merged. To do this, you try to simultaneously move the bunches closer together, while shrinking the size of their available neighbourhoods.

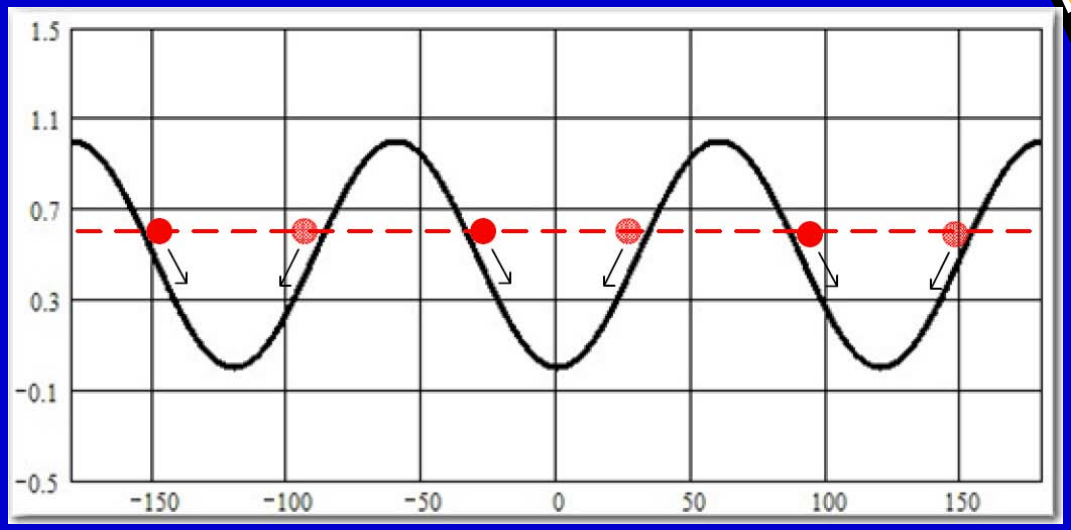


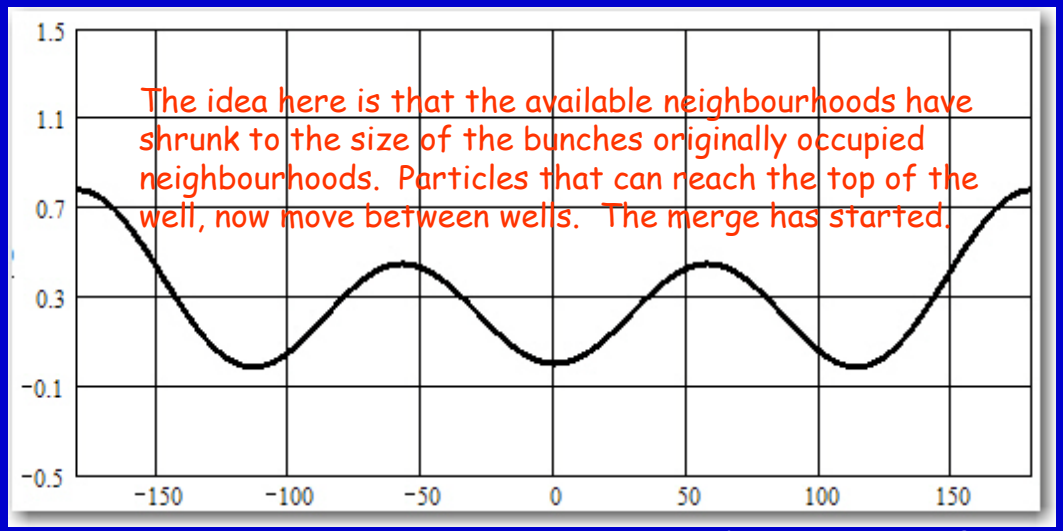
Numbers like "+2" just indicate relative amplitude. This is an exaggerated case.

h = 4 at "+2"

h = 8 at "-2"

h = 12 at "+5"

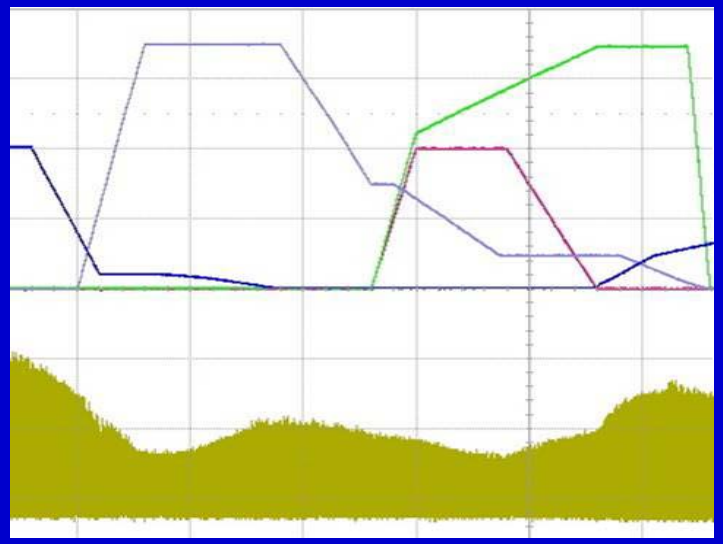




Once the merge has begun, the trick then is to keep adjusting the relative amplitudes of the different harmonics in the RF to sort of keep picture two, but just keep scaling the size of the individual wells down until you end up with just a single broad well (now at h=4).

RF Voltages

Wall Current Monitor



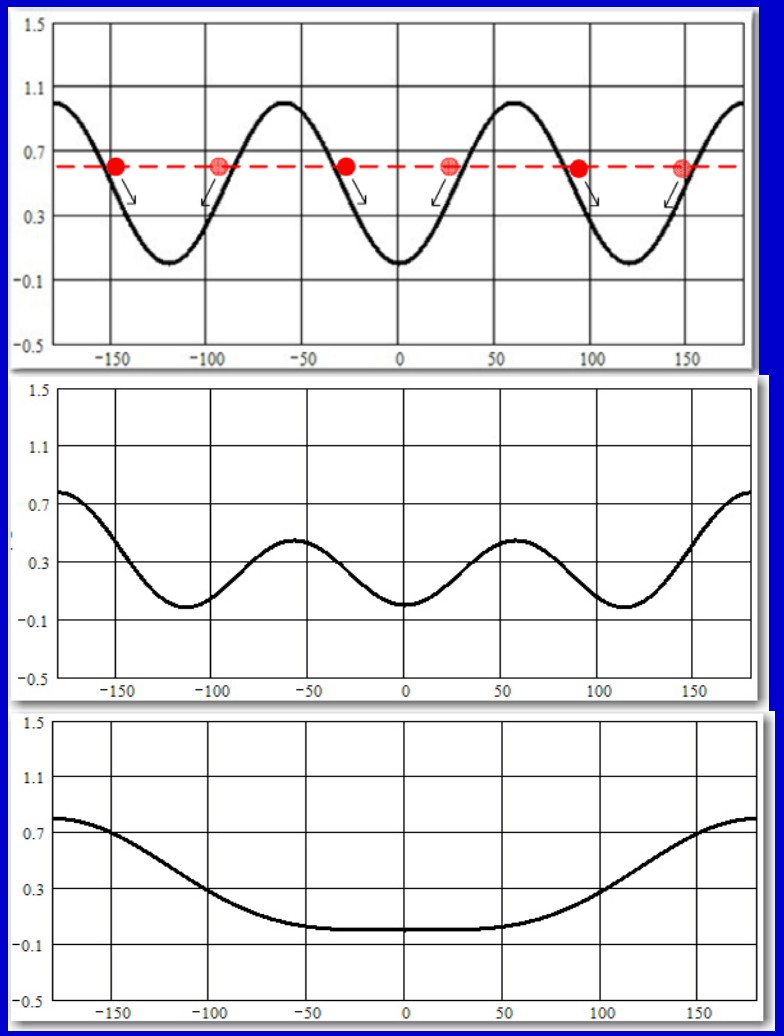
Time =>
50ms/div

^ ^
We are here.
We were there.

h = 4 at "+6"

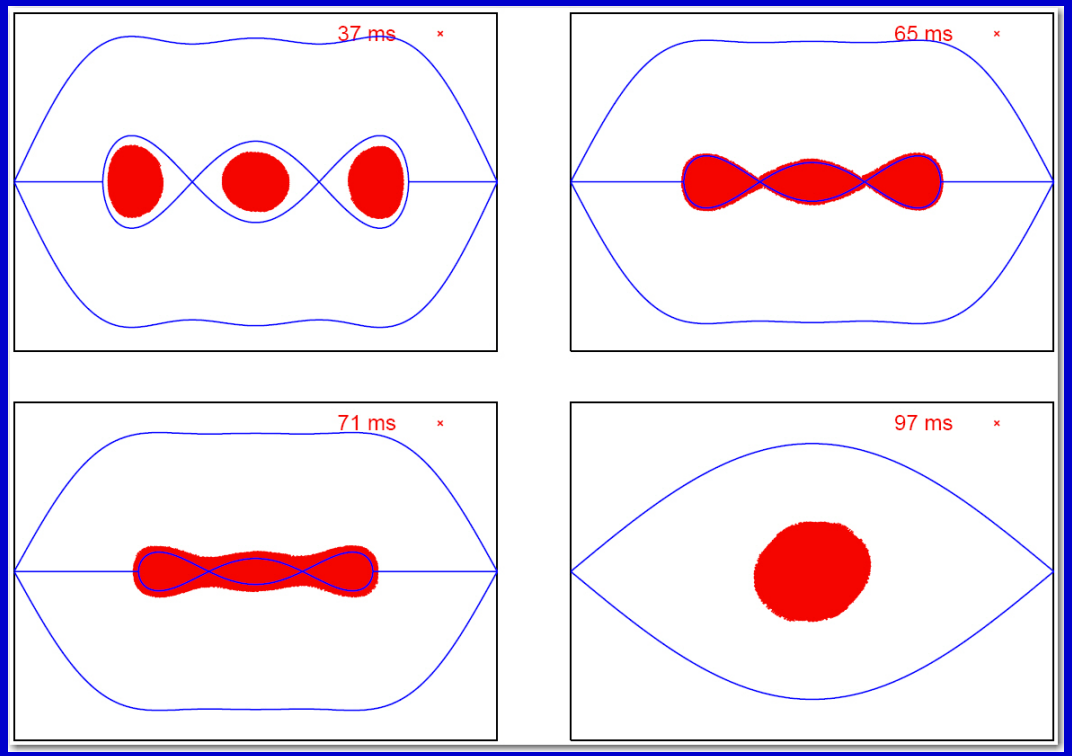
h = 8 at "-2"

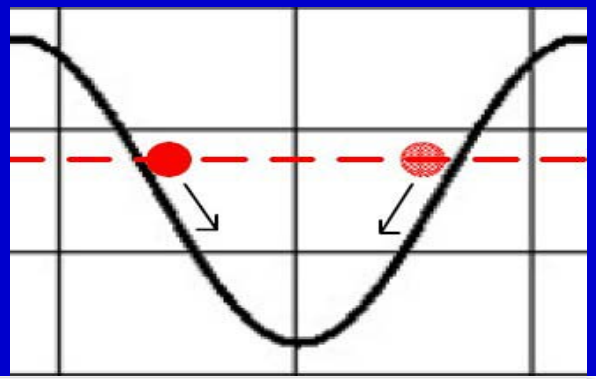
h = 12 at "+0"

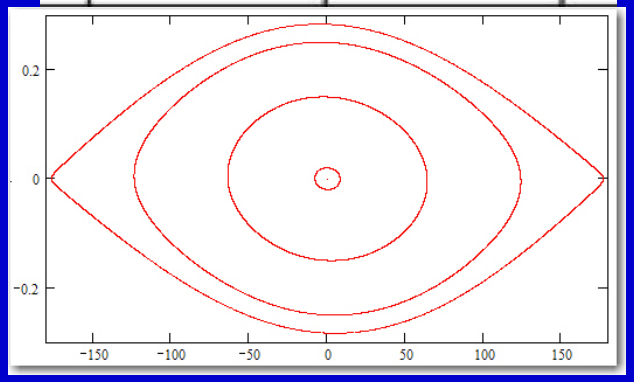


The aforementioned phase space pictures …

These pictures try to represent the location of all particles in the bunch at a particular instant in time (snapshot). The kind of coordinates used can vary, but they're all related. Here, the vertical coordinate is the particle's (relative) energy error. The horizontal coordinate is phase (or time).





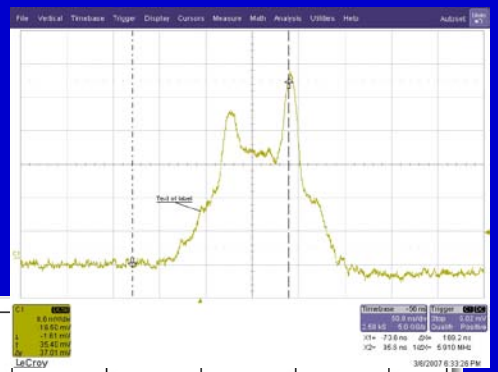


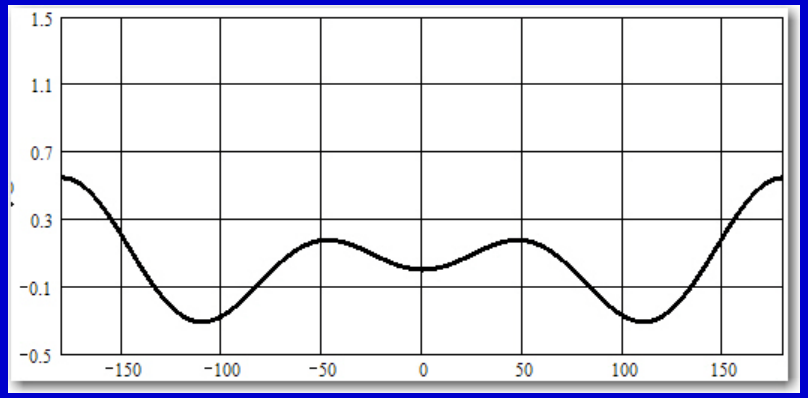
The set of four phase space plots here are a simulation of a good 3:1 merge.

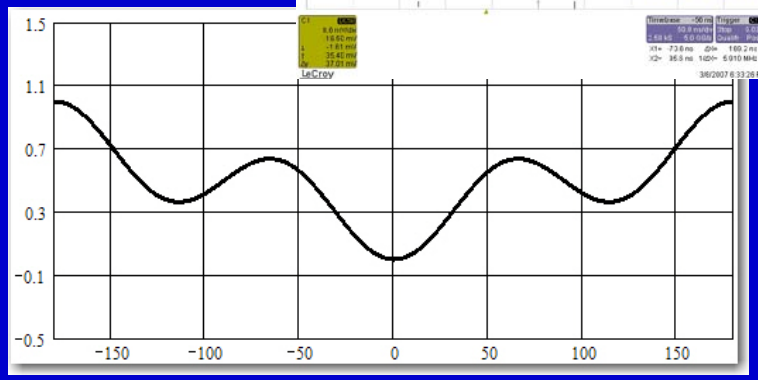
The area bounded by one of these trajectories goes like dE*dt, and when we change things adiabatically, we preserve that area.

Many things can go wrong as you try to manipulate the various harmonics. Inevitably, these will all produce a final bunch whose neighbourhood = emittance = phase space area is bigger than the sum of the original areas. This is emittance growth and we try hard to avoid it, but it can be difficult.

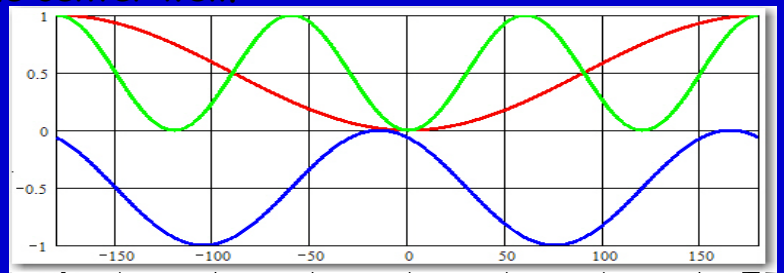
Too much h=8 raises the center well relative to the outside wells. ->



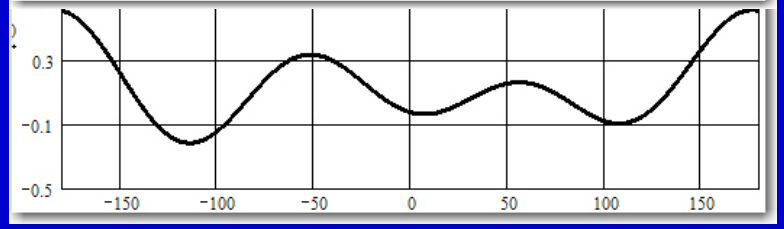




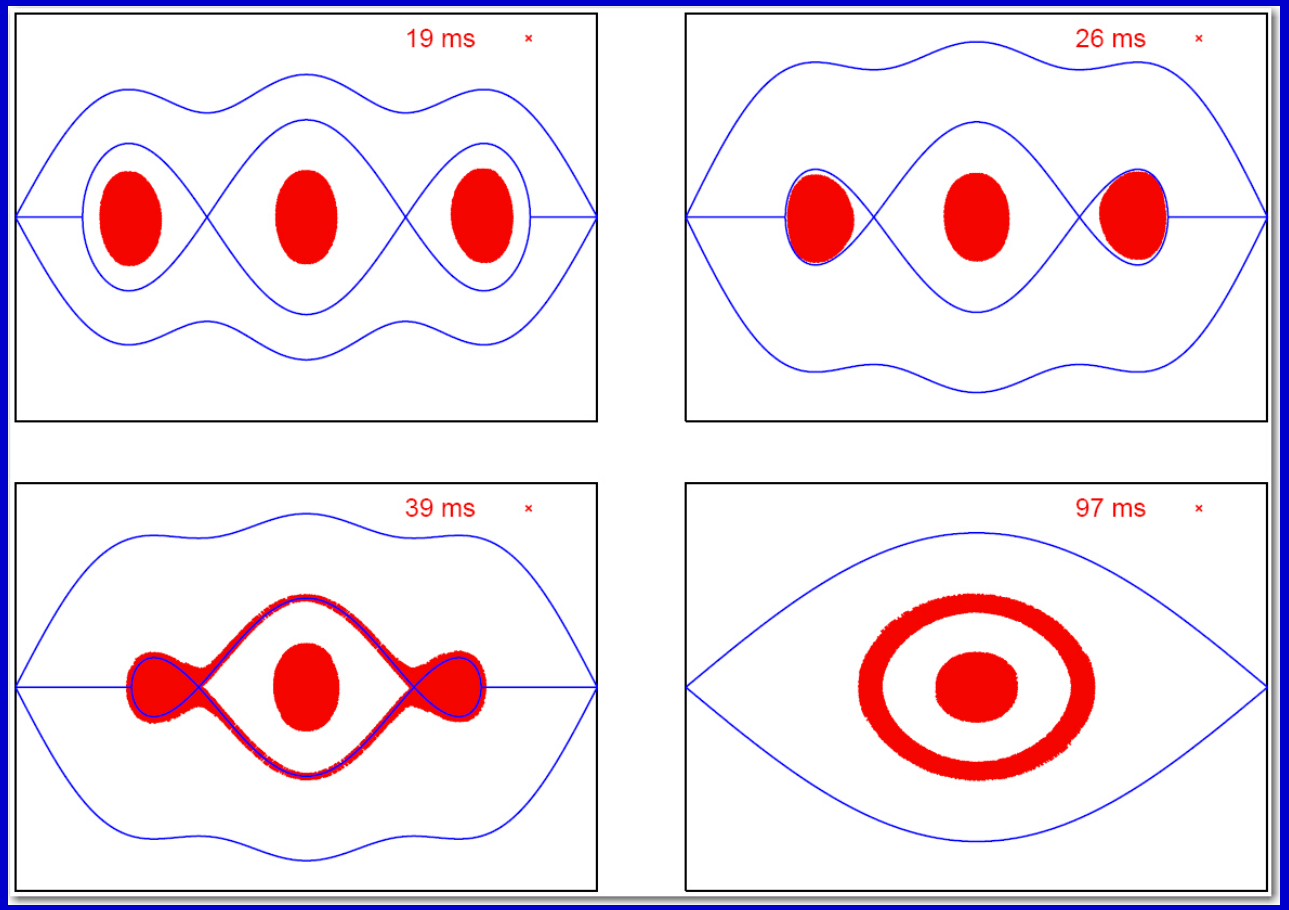
<- Too much h=4 raises the outside wells relative to the center well.

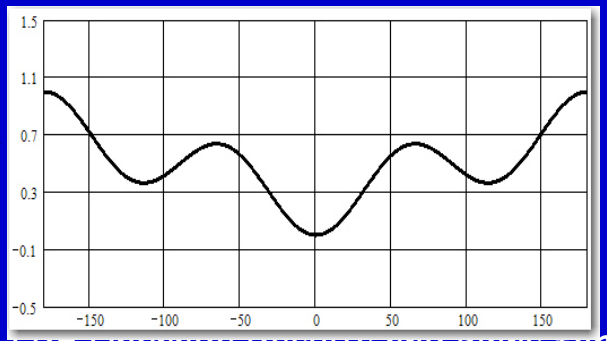


Improper h=8 phasing produces an asymmetric merge. ->



Phase space plots for a not so good merge …

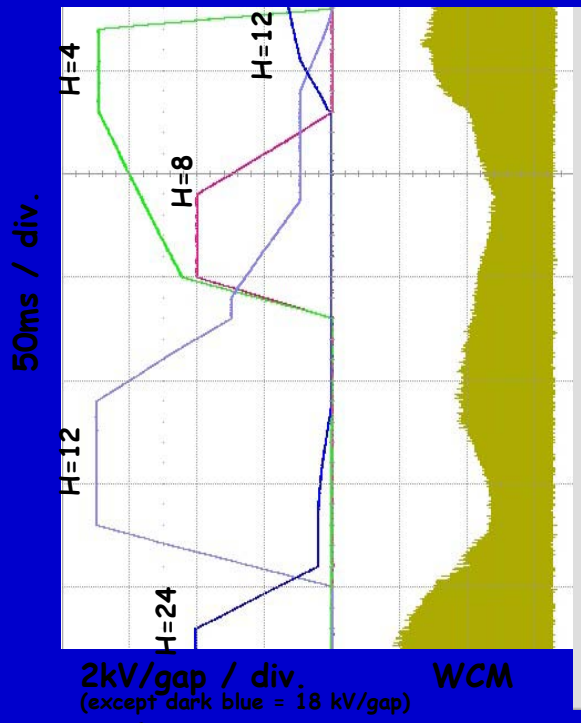


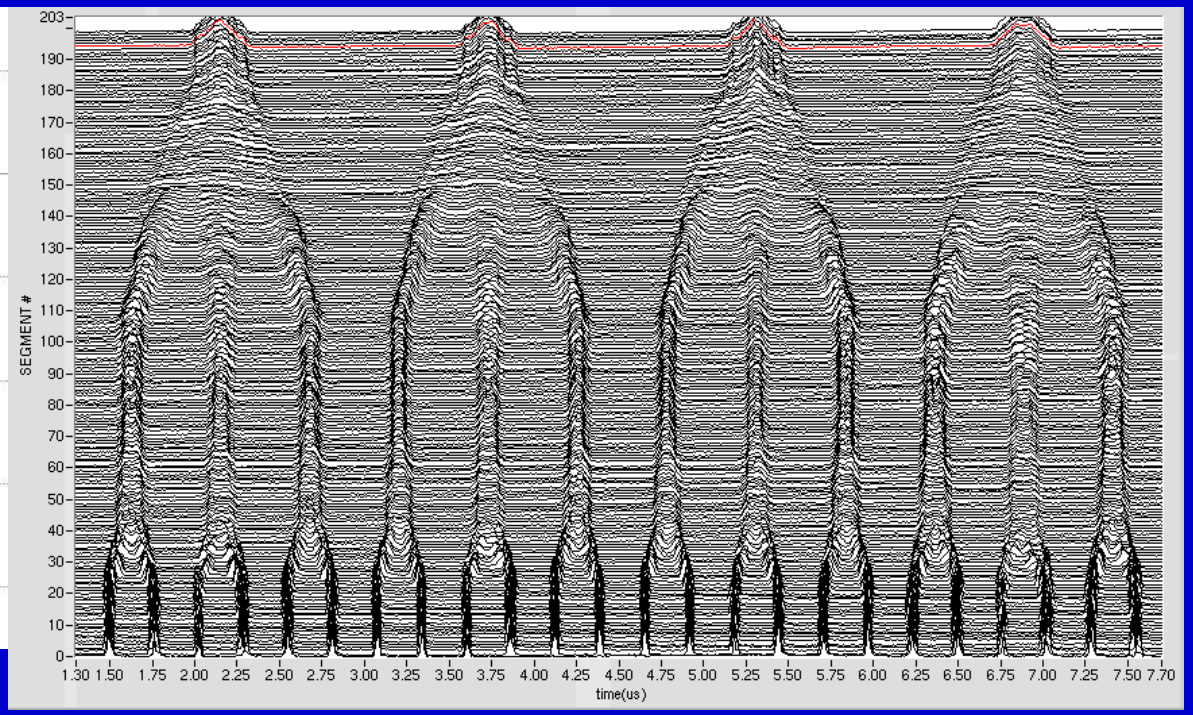


Because we have too much h=4 relative to h=8, particles in the outer wells flow over the top of the wells, down thru the center, and back up over the top of the opposite well – over and over and over …

Which brings us back to a sort of graphical representation from the beginning.

This is a decent looking 2:1 merge followed by a 3:1 merge, so long as you don't look too closely.

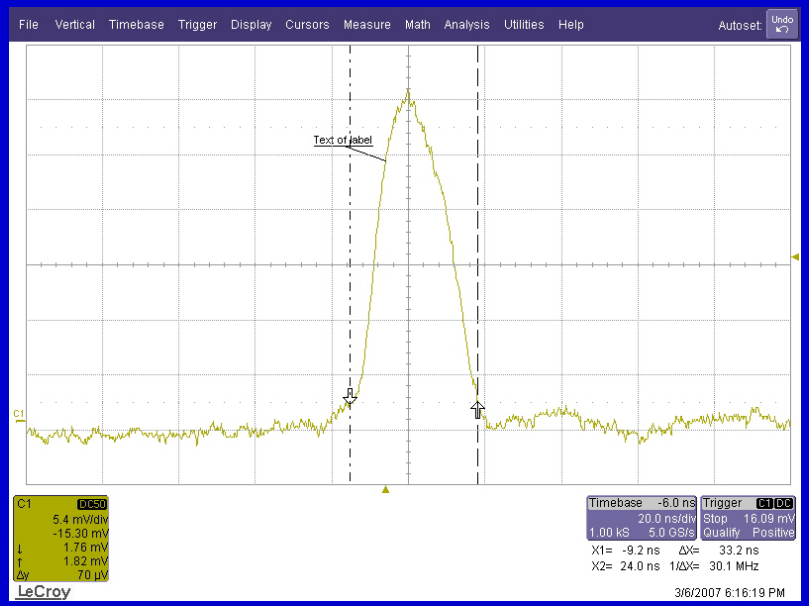




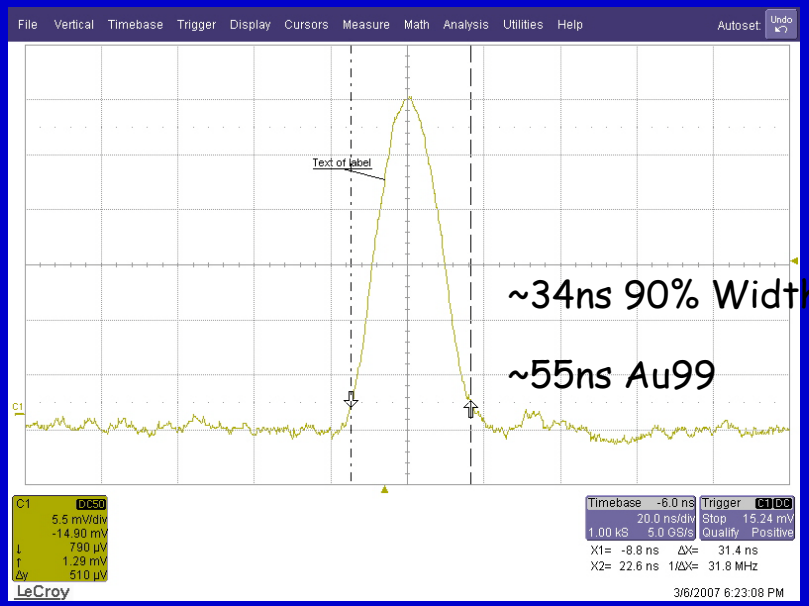
- "Mountain Range" Plot

Injected Bunches

First Turn



First Turn + 198ms



2007: $e_{1b(inj)}$ = 0.00666… eV*s/n, dP/P = 0.63E-3, Vrf = 144 kV

$e_{6b(inj)}$ = 0.04 eV*s/n

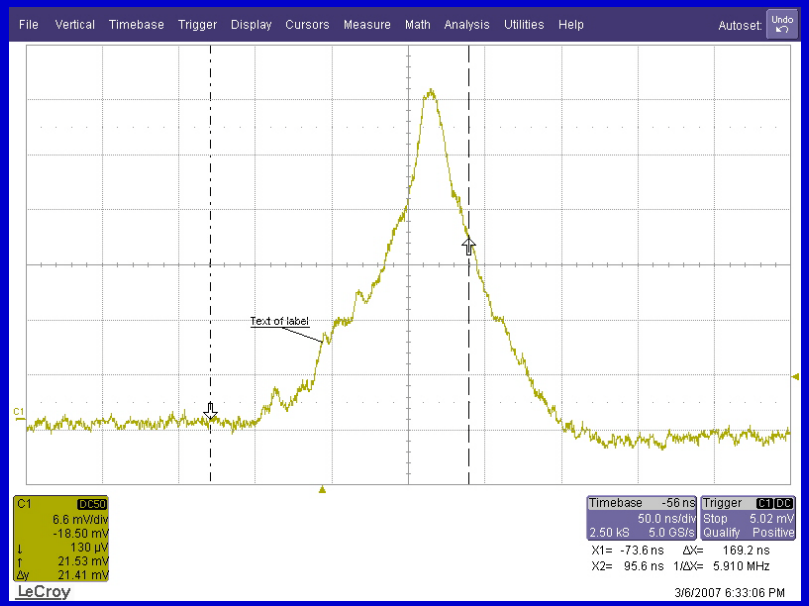
1999: $e_{1b(inj)}$ = 0.024 eV*s/n, dP/P = 1.54E-3, Vrf = 310 kV

$e_{6b(inj)}$ = 0.144 eV*s/n

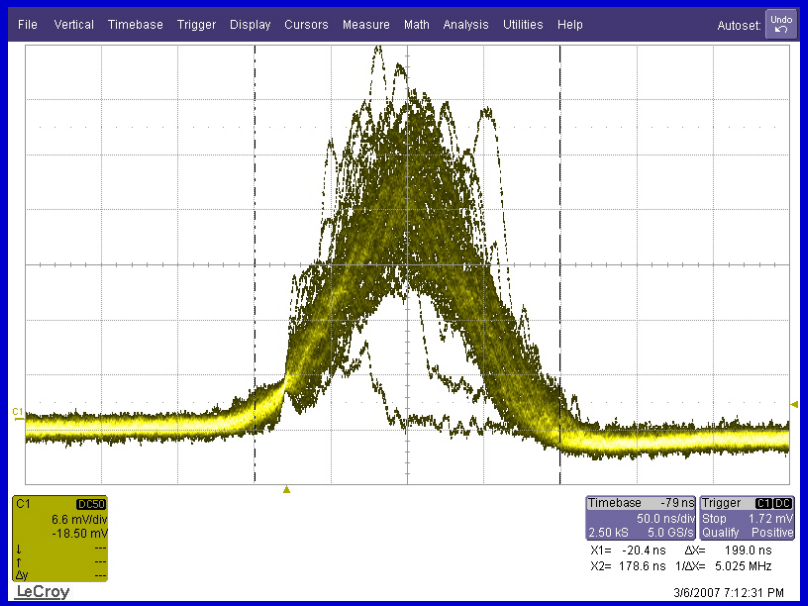
(All numbers based on equilibrium "90% width")

Bunches Post-Merge

One Shot



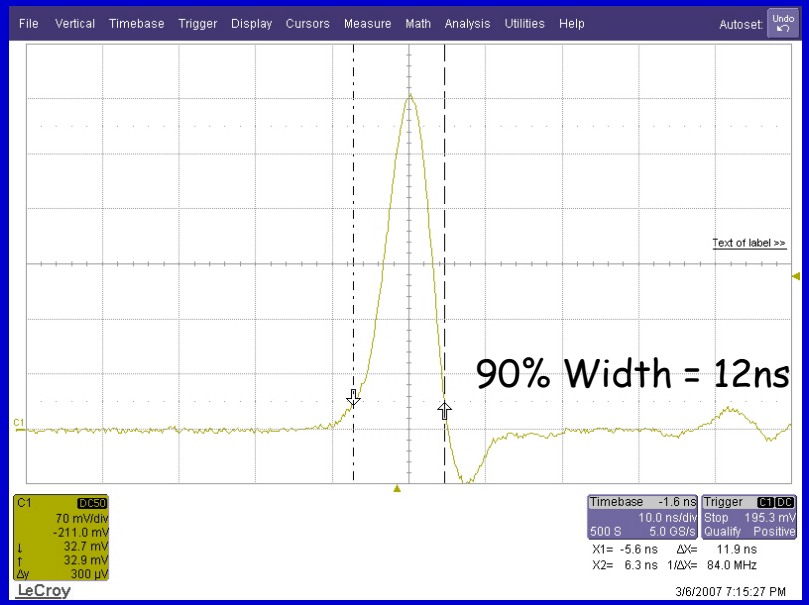
~50 Shot Persistence

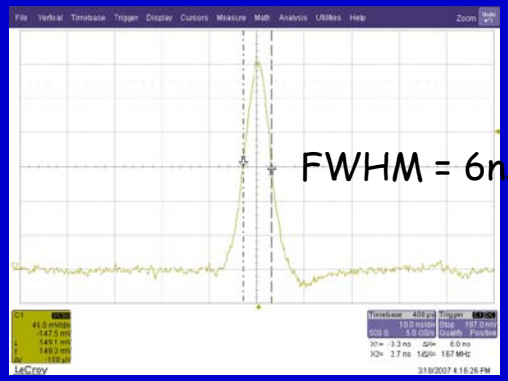


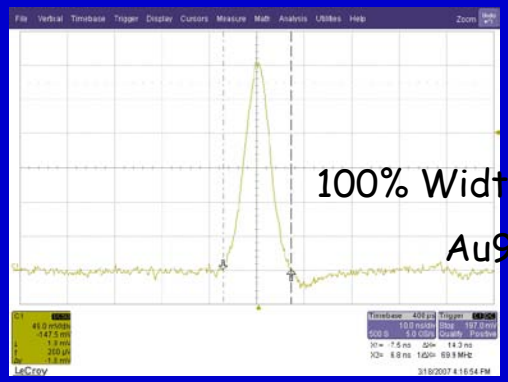
Clearly the merge is occurring with less than textbook precision.

I *think* that a.t.m., the biggest contributors to this mess are the longitudinal dipole oscillations in the bunches coming into the merge. Large shot to shot and bunch to bunch variation. The amplitude of these oscillations determines when a given bunch will start its merge action. Nonetheless …

AGS Extraction







2007: $e_{1b(ext)}$ = 0.148 eV*s/n, dP/P = 0.80E-3, Vrf = 216 kV

$e_{1b(ext)}$ / $e_{6b(inj)}$ = 3.7

$e_{1b(ext)}$ = 0.200 eV*s/n (Full Width)

1999: $e_{1b(ext\_Au04)}$ = 0.41 eV*s/n, dP/P = 1.15E-3, Vrf = 262 kV

$e_{1b(ext\_Au07)}$ / $e_{1b(ext\_Au04)}$ = 0.49 (Full width comparison)