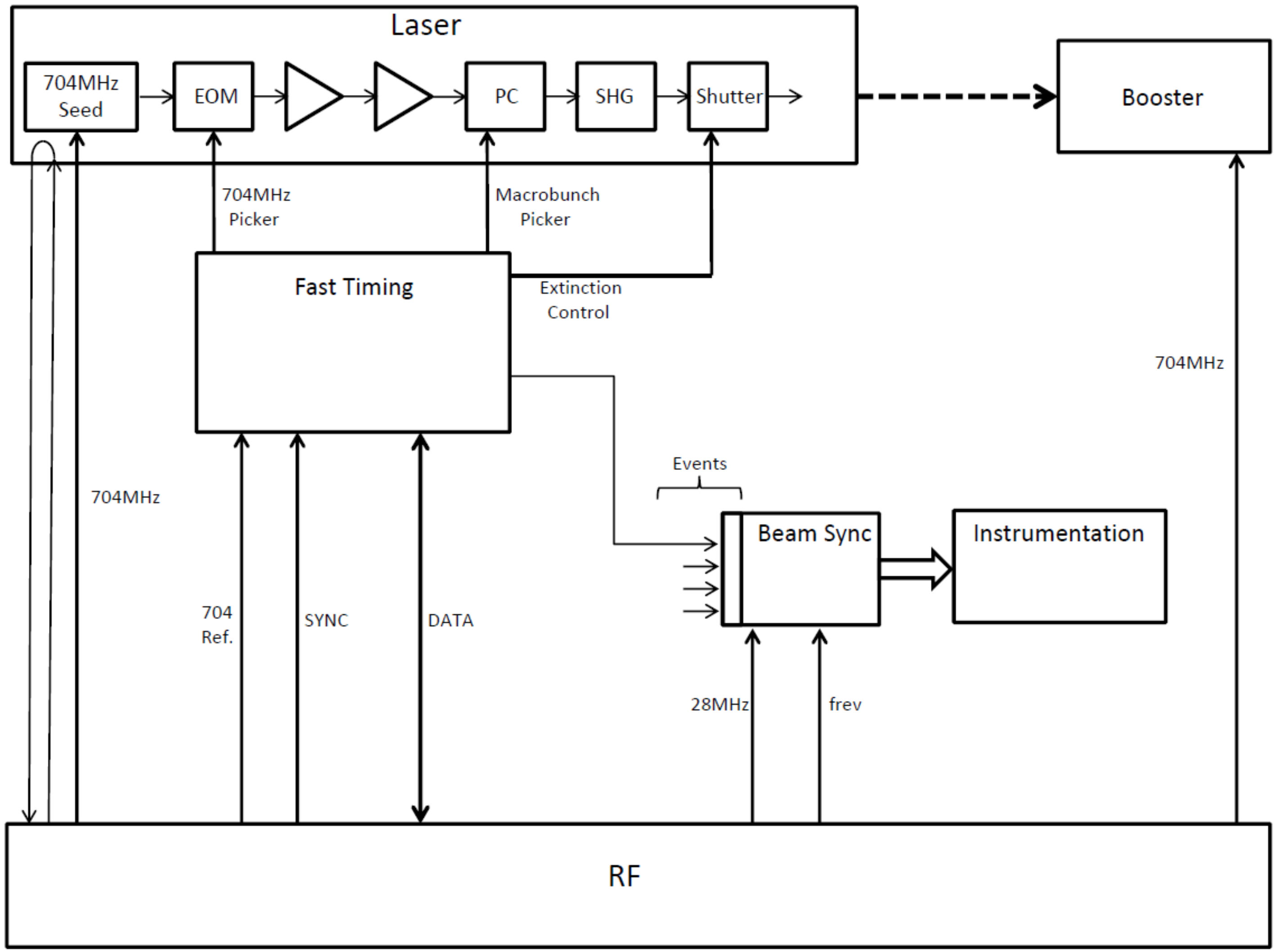
LEReC Timing

December 12, 2016

Overview

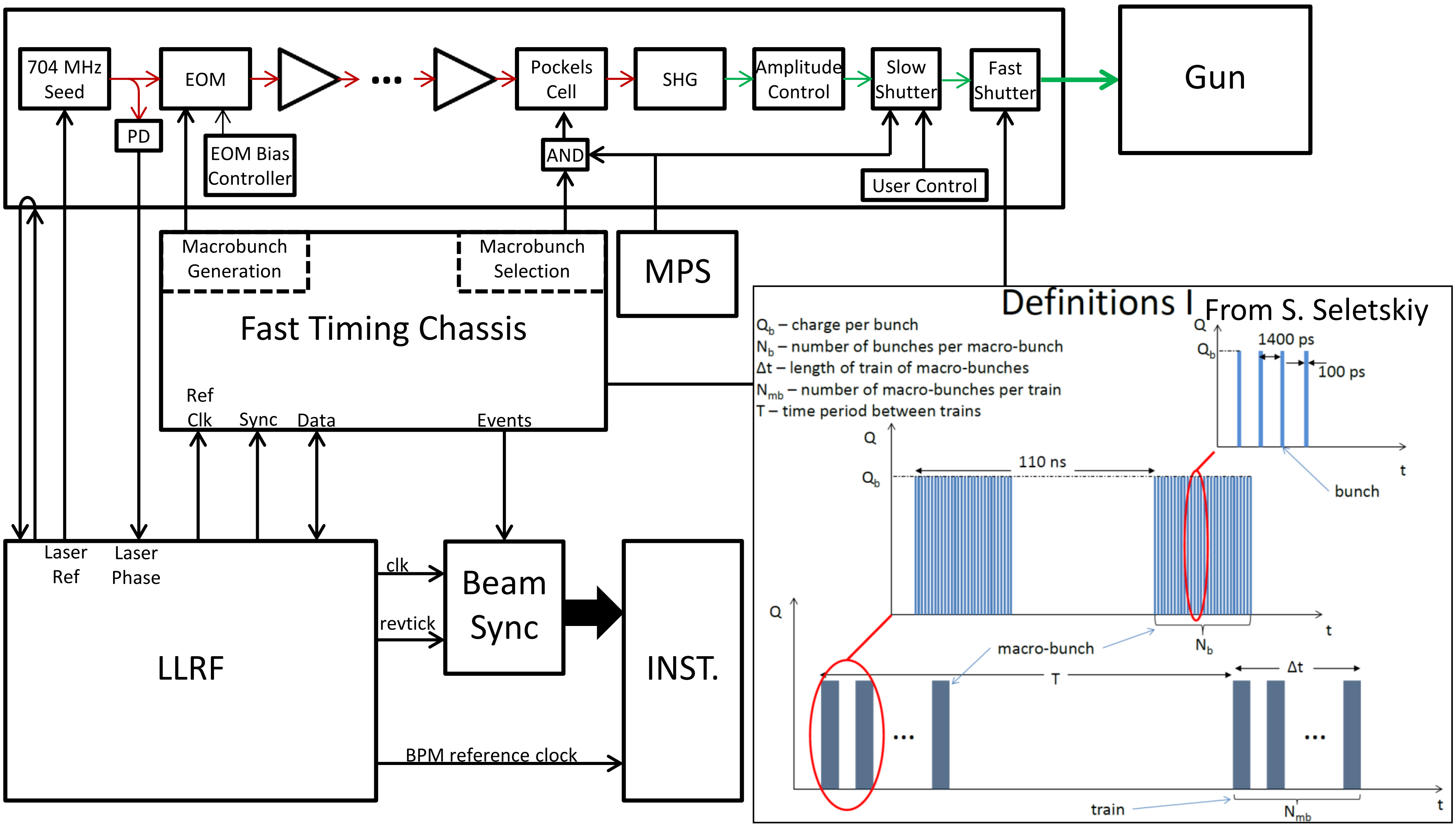
- Timing system design has more or less evolved into two separate systems: the “fast timing” system for the laser timing and the “beam sync” system for instrumentation.
- This plan still seems to make sense with some minor deviations included (for example, adding a direct reference clock sent from the LLRF to the BPM system).
- The goal of this meeting is to go over the overall system requirements one last time, and to provide an informal review to make sure what we are building for this run will meet all requirements.

Overall System Block Diagram



* This is an early version, but the basic idea is still correct

Block Diagram 2



Laser Timing Components

- EOM (electro-optical modulator)
  - Generates the 9 MHz macrobunch structure
  - Needs fast control synchronized with 704 MHz laser oscillator
- Pockels cell
  - Generates the train structure
  - With the current laser design, this allows a 1 Hz repetition rate with train lengths up to 50 ms (5% duty cycle limit)
- Fast shutter
  - In early discussions, this was included to increase laser extinction due to finite contrast of the PC
  - Are we still planning to use this for that purpose?

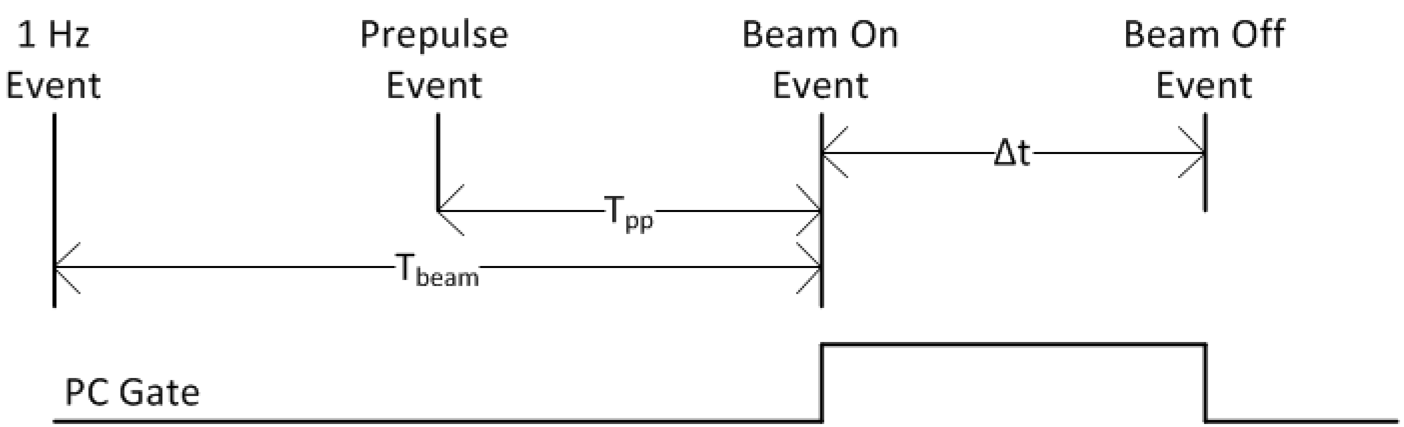
Timing Numerology

- For cooling, the electron bunch repetition rate must be a harmonic of the RHIC revolution frequency, and the macrobunch repetition rate must match the RHIC bunch spacing. It is also limited by the tuning range of the laser and RF cavities.
- For the DC Gun test this year, we can pick any frequencies we want (within reason).
- The harmonics for cooling do not have any nice common factors, but picking a bunch frequency that is a multiple (x75) of the macrobunch frequency allows us to use an interim timing system (with reduced features) for the beginning of this run.

	1.6 MeV	**2.6 MeV**	**DC Gun test**
KE (MeV)	1.6	2.6	
gamma	4.1	6.1	
beta	0.9702	0.9864	
f_rev	75870.72	77134.21	78222.22
h_macro	120	120	120
f_macro	9.104E+6	9.256E+6	9.387E+6
h_beamsync	360	360	360
f_beamsync	27.313E+6	27.768E+6	28.160E+6
h_laser	9279	9127	9000
f_laser	704.004E+6	704.004E+6	704.000E+6

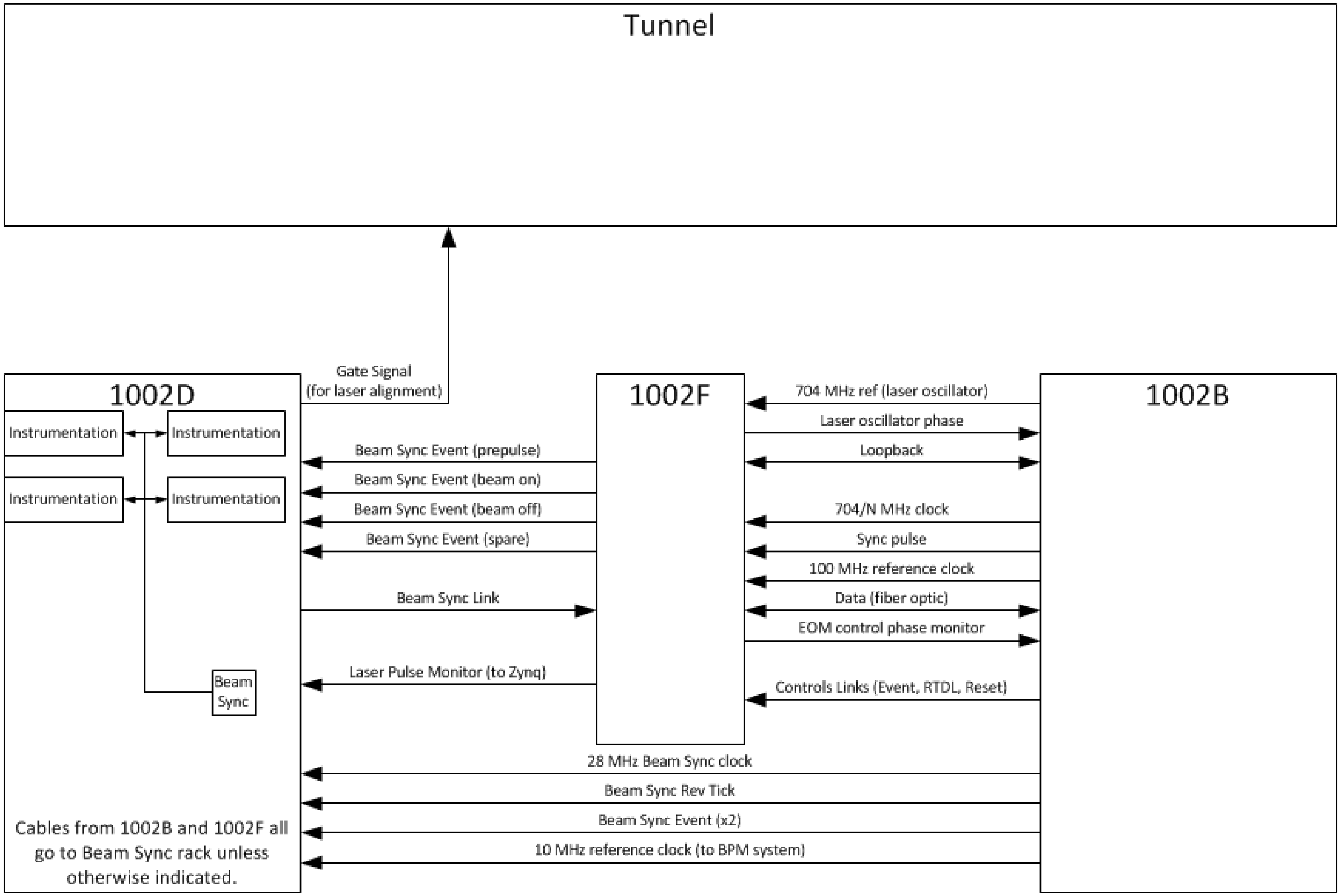
Timing System Events

- All events will be sync'ed to the RHIC Event Link 1 Hz event
- Three events will be encoded onto the LEReC Beam Sync Link: prepulse, beam_on, and beam_off
- T_{beam} and T_{pp} will be constants, Δt will be a parameter in the timing manager software
- Instrumentation that needs a pre-beam reset or arm signal will use a trigger delayed from prepulse
- Measurement triggers could be derived from either prepulse or beam_on events (qualified by Beam Sync rev_tick event)



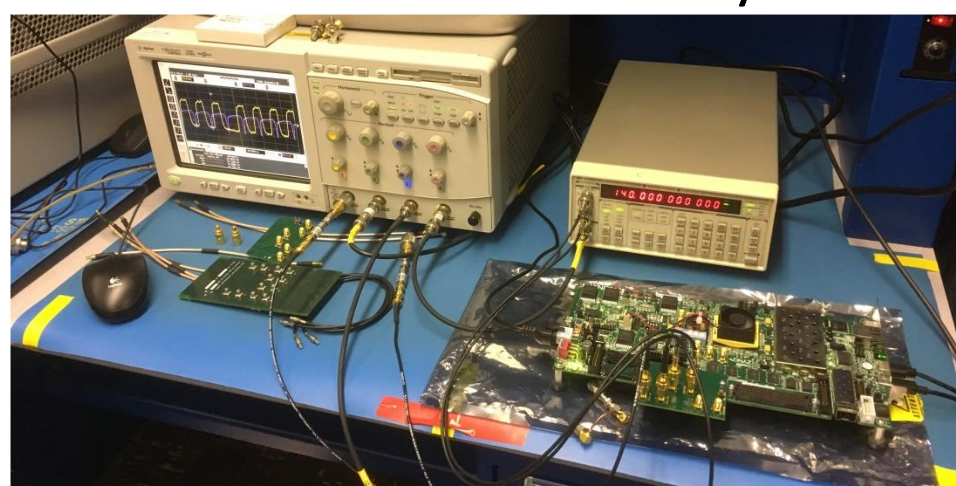
T = 1s,   106 ns ≤ Δt ≤ 50 ms

Timing System Interconnect



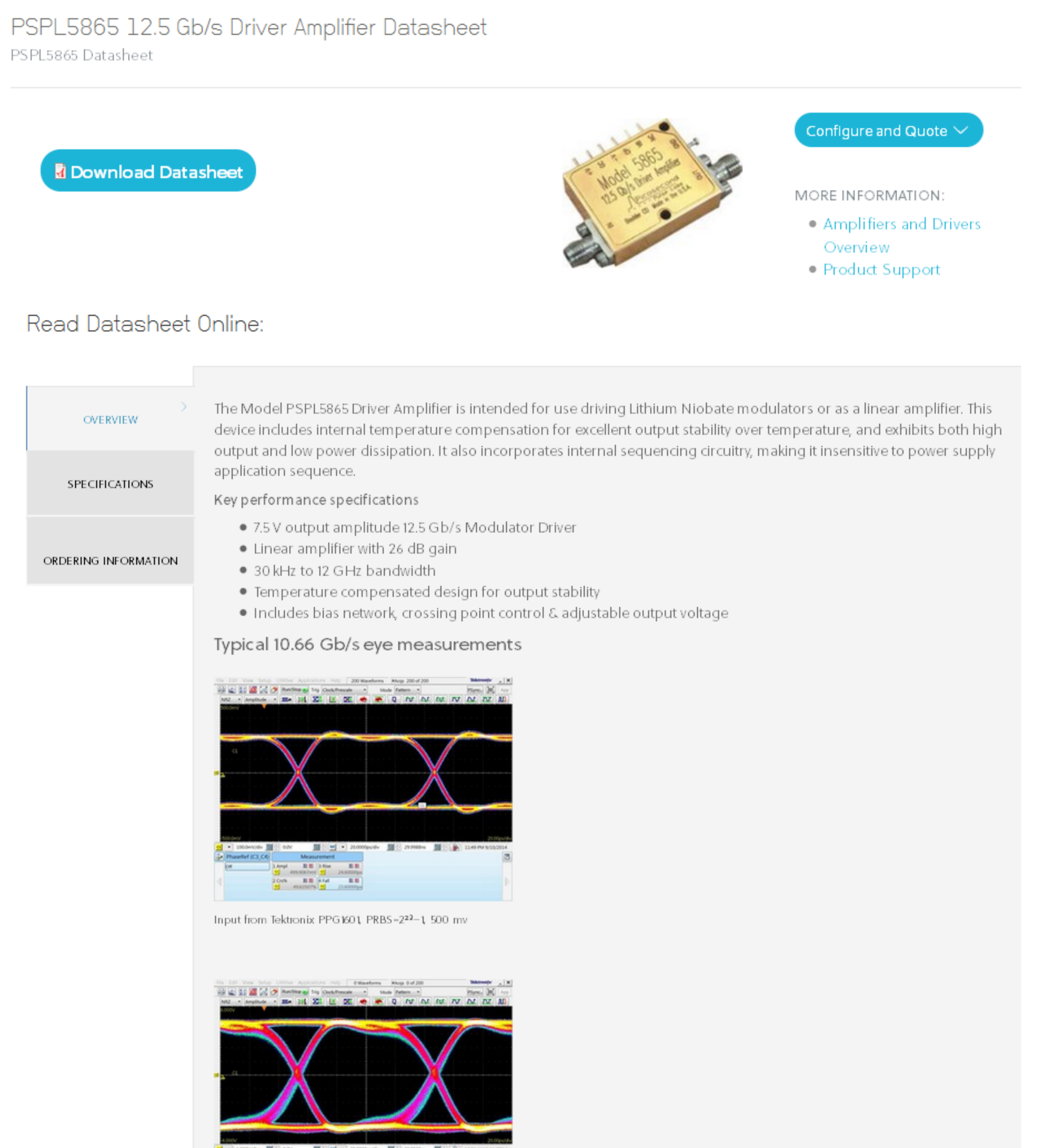
Zynq-based Controller

- We are basing the fast timing system on a Xilinx ZC706 Zynq evaluation board.
- One of the multi-gigabit transceivers (MGTs) is being used to generate the EOM gate signal. It incorporates many nice features which allow us to generate the necessary fast signal synchronized with an external clock reference.
- Also provides significant processing power and many inputs/outputs for other necessary features.
- A custom FMC daughtercard is being designed to provide the interface between the ZC706 and the rest of the system
- A designer has been assigned and the schematic for the daughtercard is nearly complete. We expect to have the boards around February.



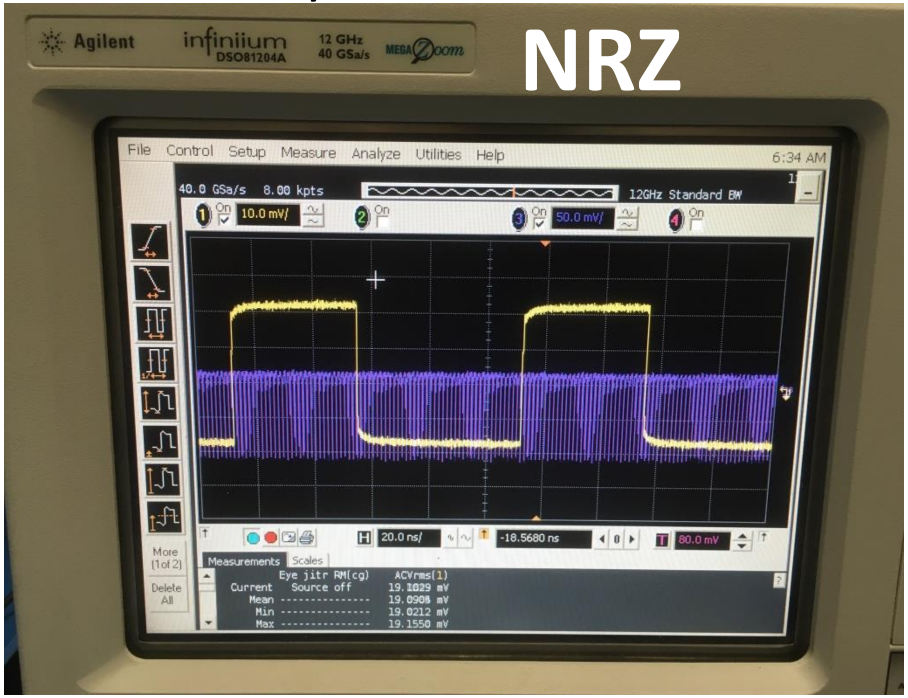
EOM Driver

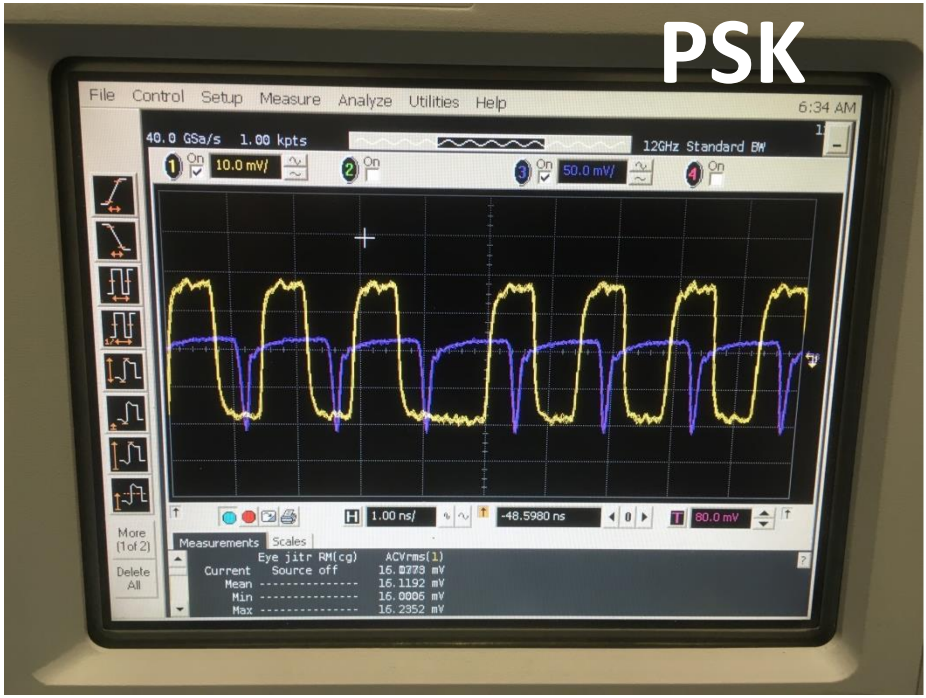
- We are using the PSPL5865 driver to provide the EOM control signal.
- This is a device designed for driving EOMs.
- It has a fast output with a large amplitude range, and a saturation mode that should make the output amplitude quite stable.



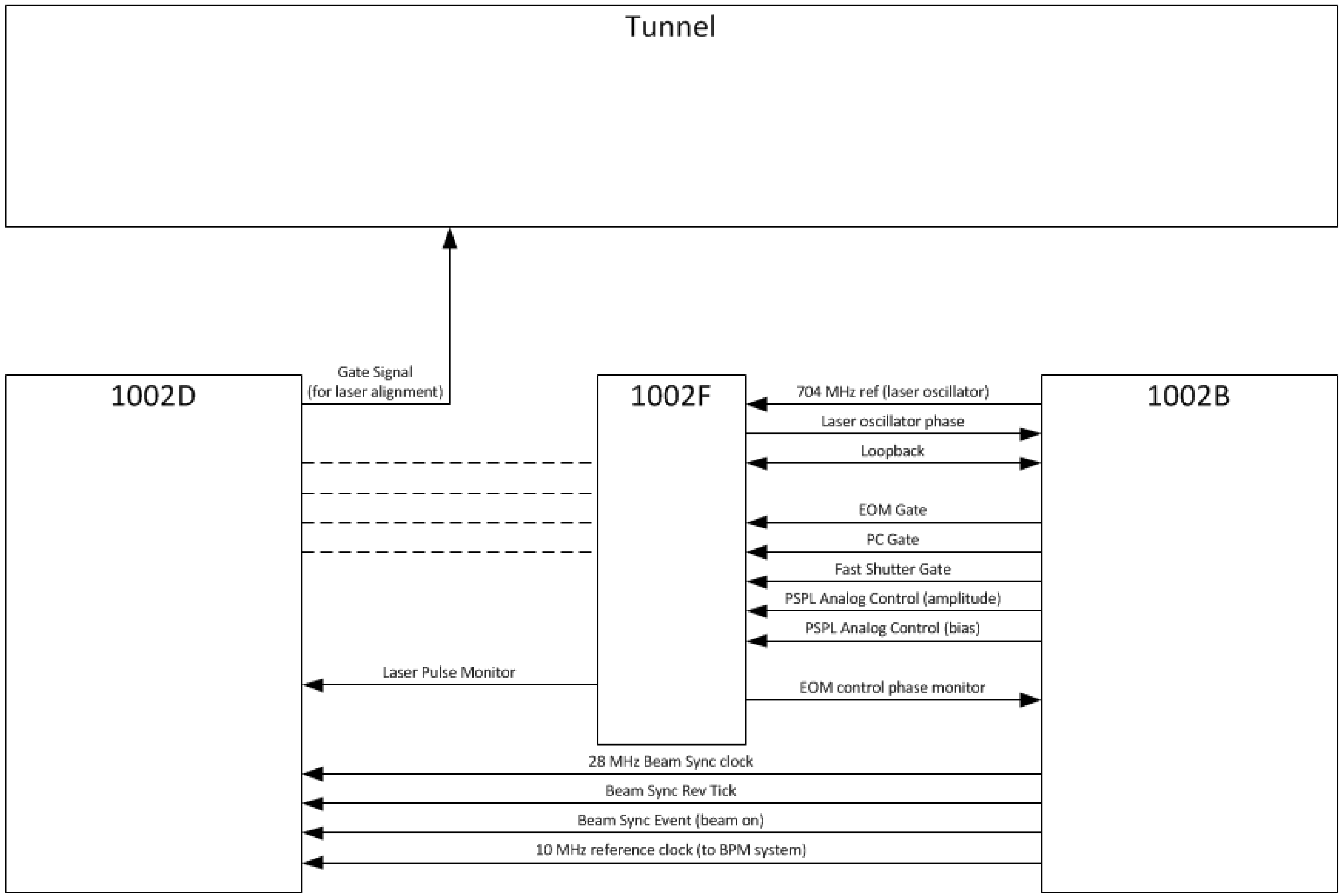
EOM On/Off Control

- We plan to support two modes for driving the EOM.
- The first is simply a 9 MHz pulse train with off and on states (similar to NRZ encoding).
- The second is generates a pulse every 704 MHz period and changes the phase of the pulse to determine on/off states (similar to PSK encoding).
- The PSK approach may have advantages for the electronics (especially power dissipation in the driver) and for amplitude stability.





Interim Timing System Interconnect



Interim Timing System Design & Limitations

- We fix the repetition rate and bunch rate harmonics to 120 and 9000.
- The EOM gate signal will come from a digital output from a LLRF DAC daughtercard. This card will use an RF synchronous clock (h=1800) to control this output. We've used similar approaches before, but for slower output signals.
- The EOM gate will only support macrobunch lengths that are multiples of 5 bunches. It will only support the NRZ mode of turning the EOM on and off.
- The Pockels cell gate and fast shutter gate will be generated either from the LLRF (in 1002B, as shown in diagram) or the Beam Sync chassis (in 1002D, using dashed lines in diagram). Fast shutter control is from a V202 channel. Pockels cell gate is from a beam synchronous source.

Instrumentation Signals

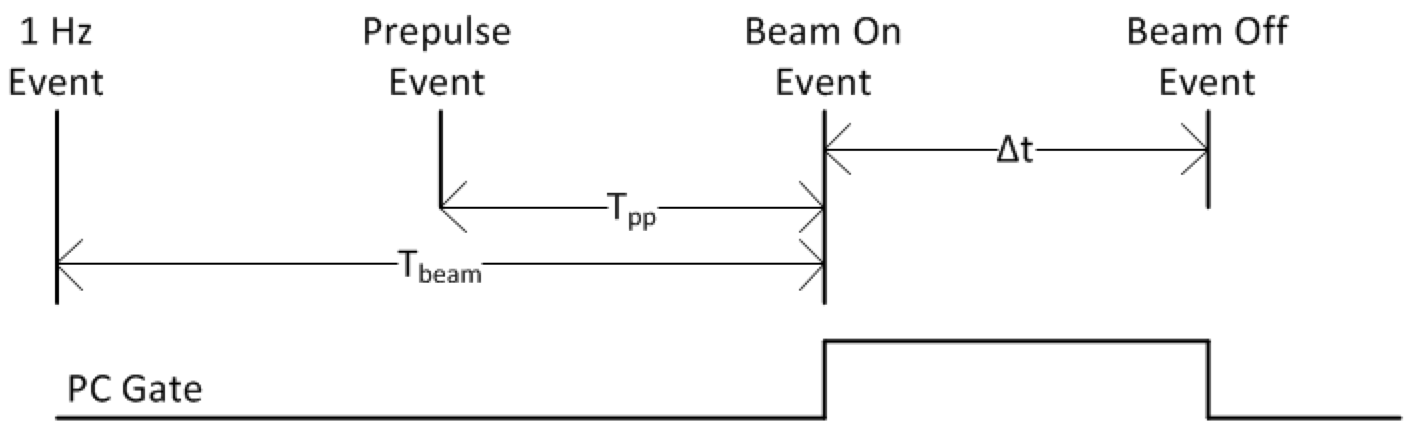
TIMING OUTPUTS		fan-outs	SOURCE
1	Zynq1 - FC's		?
2	Zynq2 - CTs		?
3	ICT trigger		V124
4	Laser Gate Detector		V124/V202
5	PMT BLM Master Gate	2	V124/V202
	PMT BLM Gate 1		
	PMT BLM Gate 2		
6	Pin Diode Scaler Reset		V124
7	Camera Master Trigger	17	V124
8	Scope Master Trigger	2	V124
	LeCroy Scope		
	Tek Scope		
9	3122 Trigger (HLX BLM)		V124
10	Libera BPM Master Trigger		V124
11	DCCT Trigger		V124
12	DCCT Gate		V124/V202
13	HLX BLM Master Reset	2	V124
	HLX BLM Reset 1		
	HLX BLM Reset 2		
14	HLX BLM Integration Gate	2	V124/V202
	HLX BLM Integration Gate 1		
	HLX BLM Integration Gate 2		
	Ion Chamber BLM (Event Trig)		EVT LINK (?)
	V301 BPM (Event Trig)		EVT LINK (?)

From T. Miller spreadsheet, **SOURCE** column added

- Assumes “trigger” or “reset” signals are short pulses
- Assumes “gate” signals must be on for as long as the beam pulse
- V124/V202 indicates using a combination of these boards to allow longer pulses than the V124 can generate (~2.3 ms)

Instrumentation Signals

- Instruments may have some combination of parameters associated with them:
  - Edge timing relative to beam (triggers)
  - Gate edges relative to beam
  - Gate widths
- Timing manager can convert these into device (V124, V202, etc.) settings



Continuous Beam Mode

- In this case, referring to a continuous train of 9 MHz macrobunches, not CW 704 MHz bunches.
- This requires laser configuration changes. (Remote?)
- The prepulse, beam on, and beam off events wouldn’t really serve any purpose.
- I assume all instrumentation that is needed for this mode must work continuously. What does this mean for the systems on the previous page that have a reset pulse or integration gate? Do they have an alternate mode for continuous operation?
- We may need to distinguish between measurements (continuous) and reporting measurements (triggered) for some devices.
- Some do have continuous mode in LEReC electronics (DCCT), some I know we use continuously in RHIC (PIN diode loss monitors), others???