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S. DeGennaro and V. Kovarik

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DATACON II BIDIRECTIONAL LINE REPEATER

Introduction

In order to facilitate Datacon II cable runs greater than two thousand feet, and to compensate for the effects of stray capacitance where multiple transceivers are paralleled across the line, a bidirectional line repeater was designed.

The repeater discriminates the polarity and duration of an incoming pulse and triggers the corresponding pulse generator (± frame pulse, ± data pulse). This restores the signal not only to the proper voltage level, but also the proper pulse width.

Therefore, a completely reconstructed pulse train is transmitted, not merely an amplified version of the incoming train.

The repeater is capable of a new transmission, in either direction, 1 μs after the termination of the previous pulse train. There is also a 1 μs delay through the repeater.

Design Considerations

In order to yield the most flexible repeater, four major specifications were considered.

1. The repeater should interface readily with the Datacon II line.
2. The repeater should be capable of operating at lower thresholds ($\sim$ 7 volts pp) than the ten volts pp usually required for reliable operation. This will allow longer cable runs, and still insure an ample margin of reliability (after a 2000' run, the signal drops to $\sim$ 12 V pp).

3. The delay from input to output should be minimized.

4. The repeater circuitry should have the capability to receive/drive multiple inputs/outputs.

These considerations are met in the following ways:

1. To simplify the interfacing, standard line driver/receiver cards are used between the Datacon II line and the repeater circuitry itself.

2. The input stage consists of voltage comparators, allowing a variable logic threshold, and increasing the sensitivity beyond the range of standard TTL logic.

3. Each bit half is reconstructed individually to produce a maximum delay of 1 μs.

4. The repeater itself is capable of receiving signals from more than one line driver/receiver card, and can also drive more than one card. This provides the capability of paralleling several units, without the problem of paralleling excessive capacitance on the input line.

Circuit Description

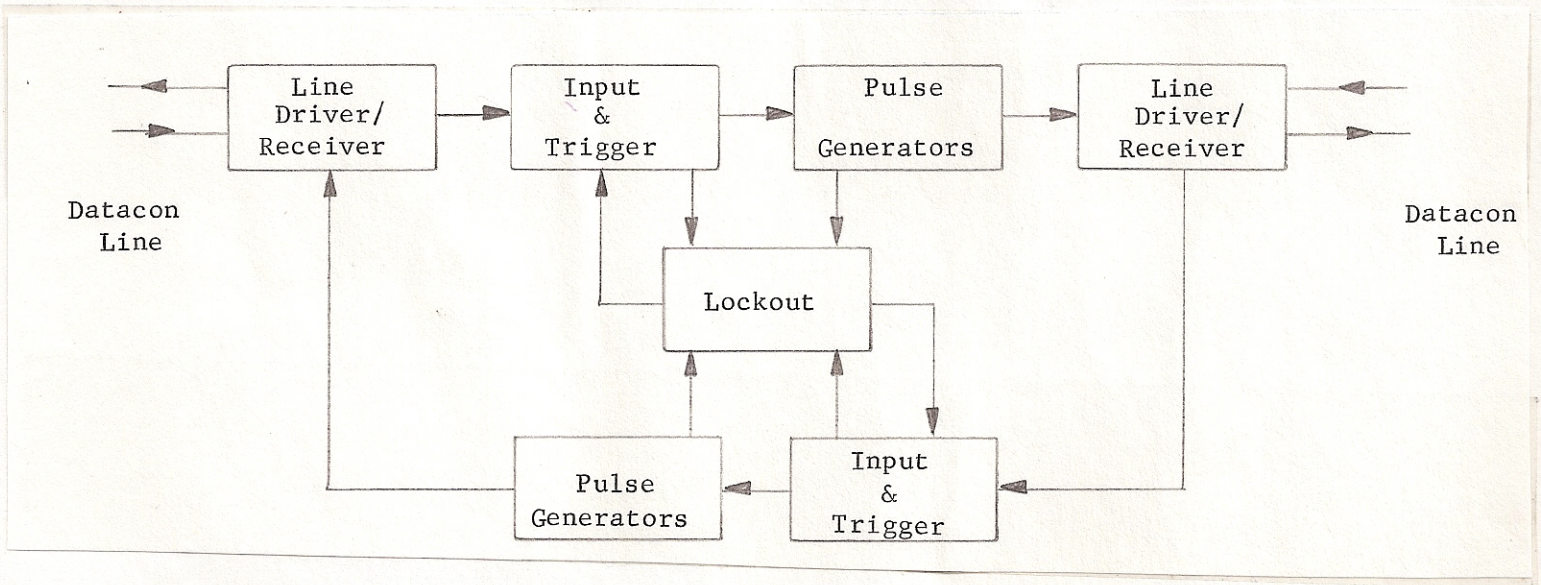

Figure 1

The repeater can be broken down into three functional subsections:

1. Input Stage

The input stage receives signals from pins 18 and 21 of the line receiver board. When a positive half pulse is received on the coax cable, a negative going pulse is produced on pin 21, alternately on pin 18 when a negative half pulse is received.

If the input pulse exceeds an internally generated 0.75 μs pulse, it is considered as part of a frame pulse. Otherwise, it is considered as part of a data pulse.

There are four mutually exclusive output lines from this portion of the circuit - one for each of the possible inputs, ± frame pulse, ± data pulse.

2. Pulse Generators

This section is triggered by the input stage and feeds the second line driver/receiver card.

The outputs drive pins 8 and 14 of the line driver board. A positive pulse on pin 8 will cause a negative pulse of equal duration to be transmitted on the Datacon line. The same pulse on pin 14 will produce a positive pulse on the line.

The four output lines from the input stage have multivibrators associated with them. When triggered, either a 1 μs (for frame pulses) or a 0.5 μs pulse (for data pulses) will be produced on pin 8 or 14, depending on the polarity of the original signal.

3. Lockout Circuit

To prevent the retriggering of one half of the repeater during transmission, the complementary half must be locked out.

A clear signal is generating by retriggering a multivibrator during transmission, and using the $\bar{Q}$ output to hold the clear inputs of the second half low. One micro-second after the transmission is completed, the $\bar{Q}$ will return high, enabling a new transmission in either direction. A more detailed description is found in the "Circuit Operation" section below.

Input Specifications

Input pins 21 and 18 are normally high ($\sim$ 4 V) and drop low, respectively, when a positive or negative pulse is received. However, as the peak-to-peak level of the Datacon II signal drops below 10 volts pp, these pulses only drop from $\sim$ 4 to $\sim$ 3 volts. This is well above the logical zero threshold of standard TTL logic, and would be the limiting factor in the repeater's response. The voltage comparator configuration shown below, allows an arbitrary logic boundary to be established.

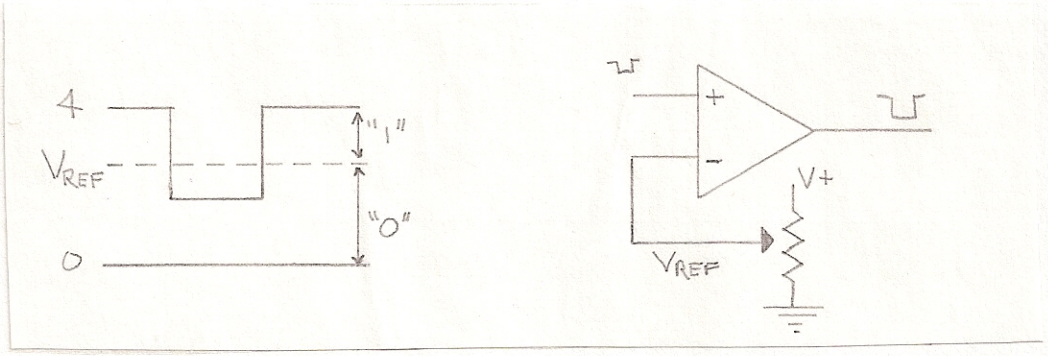

Figure 2.

Normally, V_{ref} should be set between 3 and 3.2 volts. This allows the extension of the repeater's range down to $\sim$ 7 volts pp in low noise environments. However, to maintain the flexibility of the repeater, this threshold can be established anywhere in the range of 0 to 4 volts. In a high noise environment, the threshold can be dropped, reducing the sensitivity. This will necessitate shorter cable runs, but will insure the proper operation of the repeater. Therefore, the repeater can respond to an input pulse between 7 and 30 volts pp.

The input pulse width also decreases with the decreasing peak-to-peak signal, and of itself is not a limiting factor. The only consequence is that when the input drops to the peak-to-peak voltage threshold, the frame pulse will no longer be distinguishable from the data pulses. In all other cases, the output pulses are independent of input pulse width.

The repeater can continually transmit pulse trains in either direction, provided that there is a minimum dead time of 1 μs between successive trains.

Output Specifications

The generated pulses meet the Datacon II specifications. Frame pulse halves are adjustable between 0.8 and 1.2 μs, data pulse halves, between 0.35 and 0.6 μs. The timing between pulses is identical to that of the input train. The output pulses are shifted 1 μs in time with respect to the input pulse train.

Multiple Input/Outputs

Inputs- More than one line driver/receiver card can feed the repeater. This may be accomplished by paralleling pins 21 and 18 of the cards and isolating them with small RC's. Should more isolation be required, multiple comparator sections can be used with the outputs fed through an AND gate to the repeater circuitry.

Outputs - The repeater logic can drive multiple line driver/receiver cards, within the fan-out restrictions of the output inverter chips. Buffers can be added for more current drive, should it be necessary.

Circuit Operation

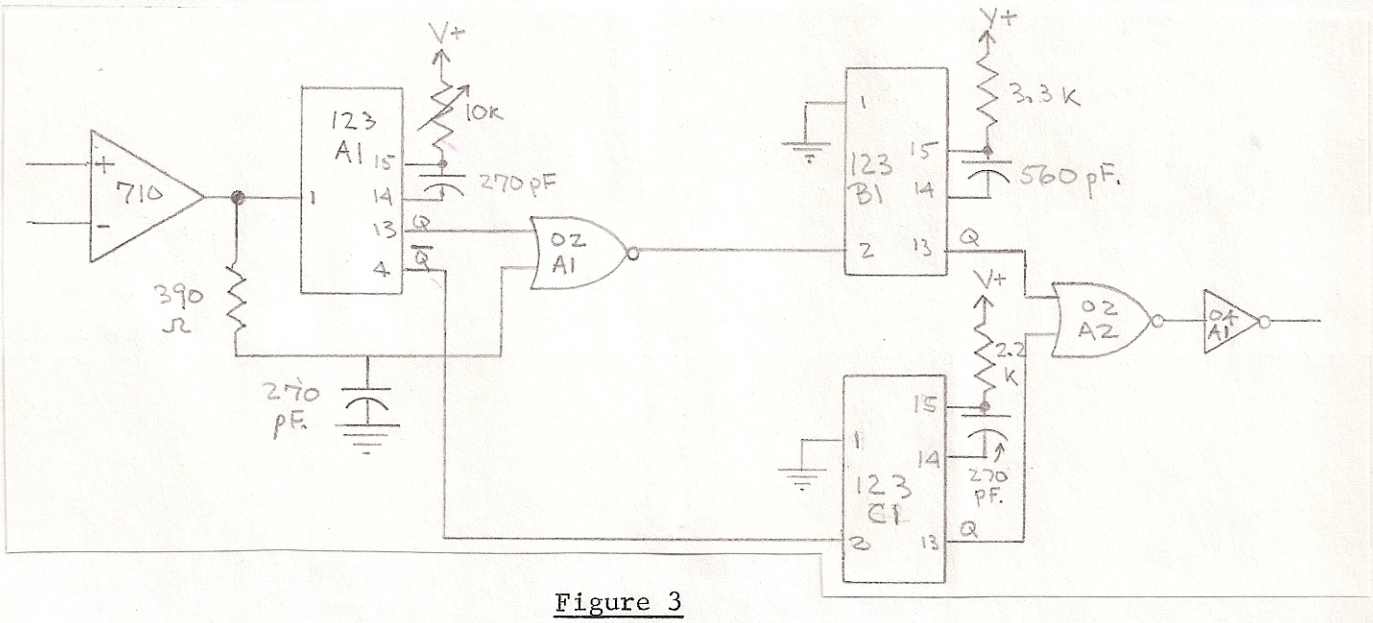

Figure 3

One quarter of the input and pulse generating circuitry is shown above.

123A1 generates the 0.75 μs comparison pulse, triggered by an incoming pulse from the voltage comparator. If the incoming pulse exceeds 0.75 μs, a positive pulse appears at 123B1/2, and triggers a 1 μs frame pulse at the Q output. In any instance, the comparison pulse itself triggers a 0.5 μs pulse at the Q output of 123C1. The Q outputs of 123B1 and 123C1 are OR'ed together, allowing the longer of these pulses (1 μs for a frame pulse, 0.5 μs for a data pulse) to pass to the second line driver/receiver board.

The timing components on 123B1 and 123C1 are nominally set for 1 μs and 0.5 μs, respectively. They can be varied to provide a range of output pulse duration, as required in any specific application.

This circuit is essentially replicated at pins 21 and 18 of each line driver/receiver board.

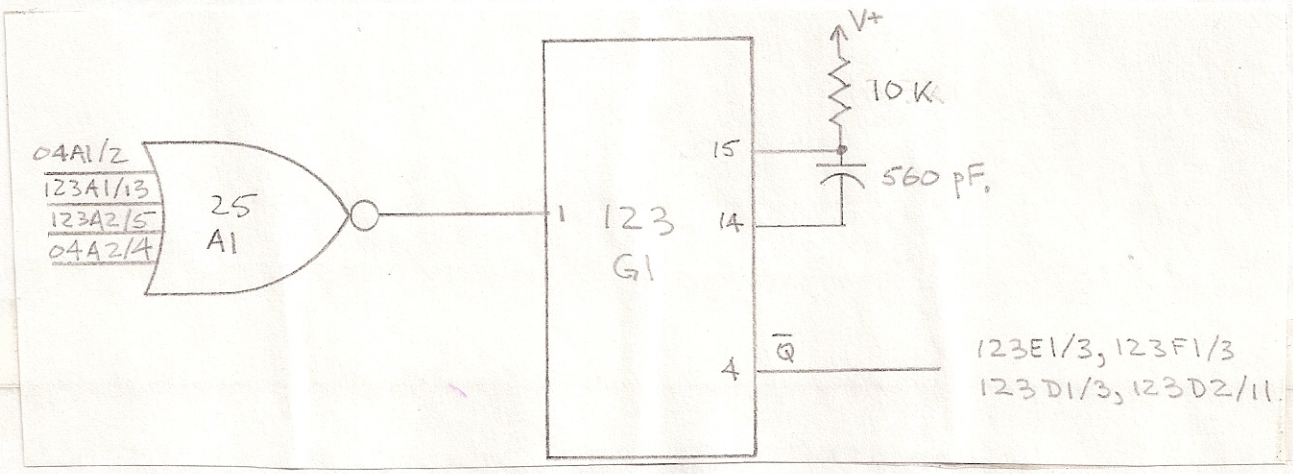

Figure 4

One half of the lockout circuitry is diagramed above. The four comparison and output pulses of one half of the repeater are tied together to provide retriggering pulses to 123G1/1. The 123 is retriggered every 0.8 μs, with an output pulse duration of 1 μs, yielding a constant low level signal at the $\bar{Q}$ output during a transmission. This disables the 123's in the second half of the repeater. Once the transmission is completed, the $\bar{Q}$ returns high, enabling either half of the repeater to initiate a new transmission.

The complete schematic is found on Drawing #D09-E713-4.

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