BROOKHAVEN NATIONAL LABORATORY
Associated Universities, Inc.
Upton, New York

EP&S DIVISION TECHNICAL NOTE

ADDENDUM to No. 58

V.J. Kovarik

January 27, 1975

Signal Specifications and Transceiver Operation for DATACON II System

Operational experience indicates that changing the allowable t_w value under Data Pulse Tolerances will improve system reliability. Page 3 of the Tech Note has been changed to reflect the new tolerance.

Former tolerance - $t_w = 0.50\ \mu sec. \pm 0.050\ \mu sec.$

New tolerance - $0.350\ \mu sec. \leq t_w \leq 0.500\ \mu sec.$

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Signal Specifications and Transceiver Operation for DATACON II System

Introduction

The following specifications have been adopted to standardize the signals on the DATACON II* coaxial transmission line. The specifications refer to a signal measured at the output of a device that is properly terminated. Figure 1 is a typical system block diagram.

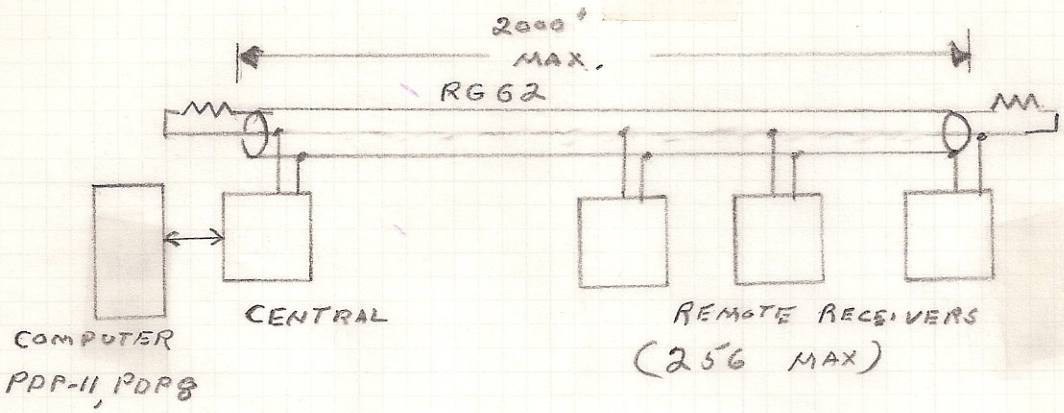

Figure 1

*DATACON II, DATACOM II, and DATACON 2 are synonymous labels.

Figure 2 shows a typical signal transmission on the line.

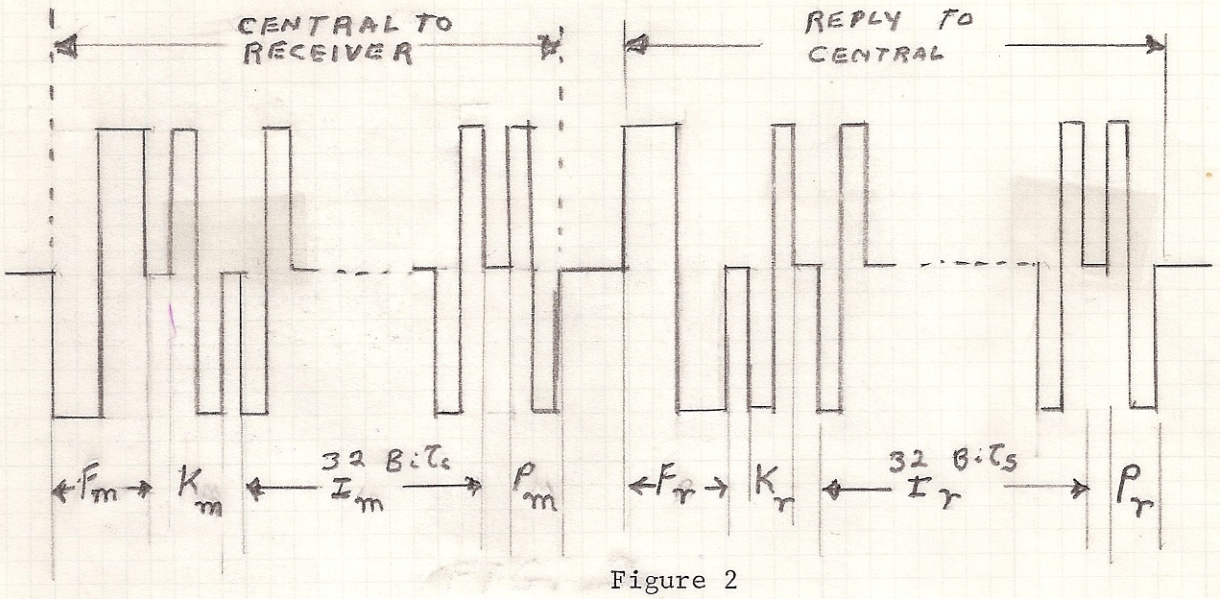

Figure 2

The functions of the signals are briefly described below:

F_m clears all receiver registers.

F_r clears central registers and locks out all other receivers.

K_m,K_r (always a logical one) indicates end of shift.

P_m,P_r parity check on data transmission.

I_m (information bits) contain the address, command and magnitude bits.

I_r (information bits) contain the magnitude, sub-address and status bits.

The minimum time for a complete transmission and reply is approximately 120 μsec. The frame signal-width is approximately 2 μsec and each data signal-width is approximately 1 μsec. The minimum deadtime between data bits is 0.55 μsec.

Specifications

Figure 3 illustrates a frame signal and a few data signals. The widths of all pulses are measured from the 10% value of E_1 to the crossover points as shown in Fig. 3.

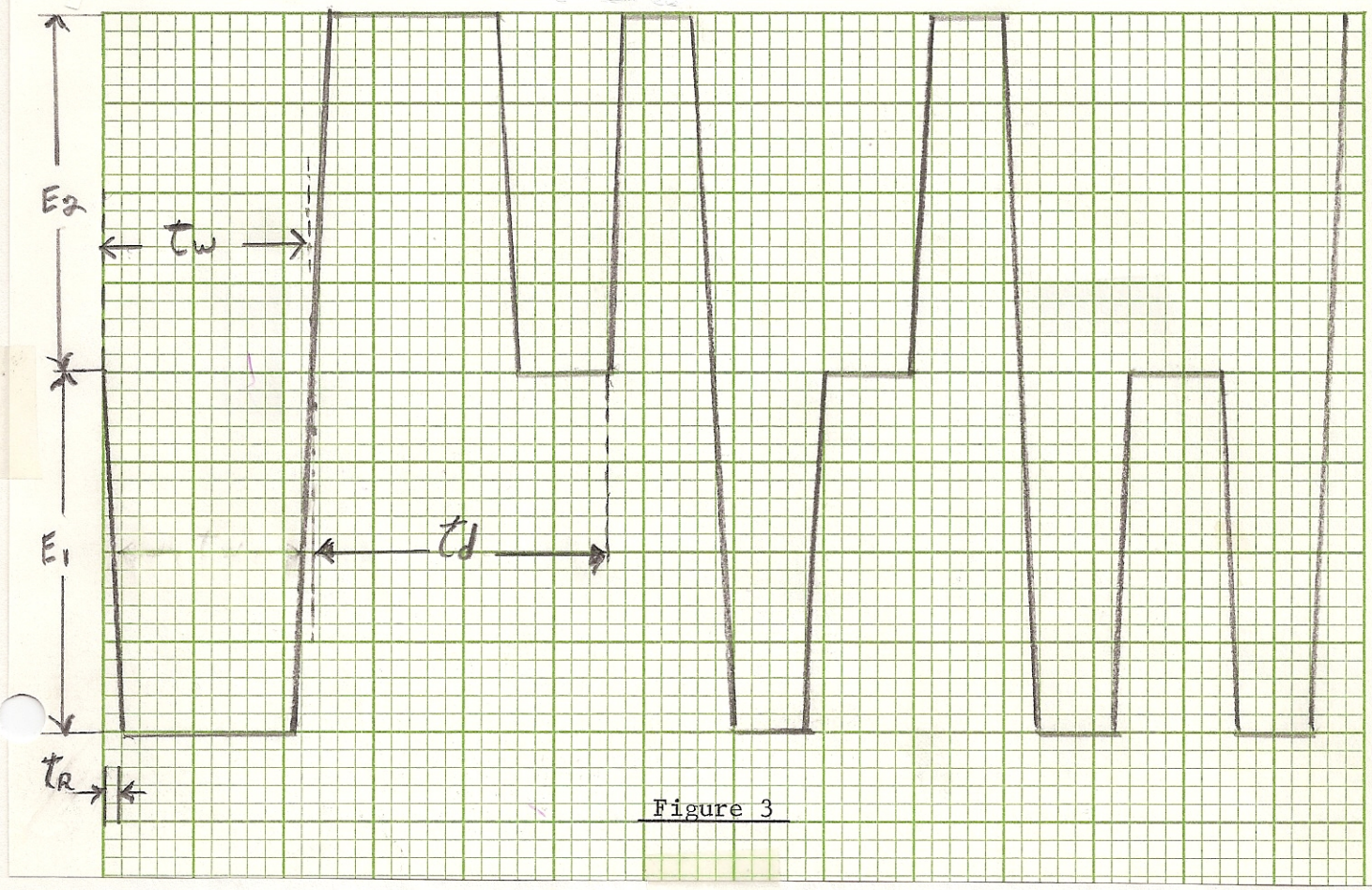

Figure 3

Frame Pulse Tolerances

t_w = 1.05 μsec ± 0.10 μsec
$t_d \geq$ 1.65 μsec
$t_r \leq$ 0.10 μsec (10% to 90%)
E_1 = 15 V ± 1 V
$E_2 = E_1 \pm 1.0\%$

Data Pulse Tolerances

0.350 μsec. $\leq t_w \leq$ 0.500 μsec.
$t_d \geq$ 1.1 μsec
$t_r \leq$ 0.10 μsec (10% to 90%)
E_1 = 15 V ± 1 V
$E_2 = E_1 \pm 1.0\%$

Transmission Tolerance

$$\frac{\left| \sum_{n=1}^{35} E_{1_n} t_{w_n} - \sum_{n=1}^{35} E_{2_n} t_{d_n} \right|}{\sum_{n=1}^{35} \left(t_{w_n} + t_{d_n} \right)} \leq \pm 0.25 \text{ V} .$$

The last requirement allows a maximum base line shift of 0.25 V at the end of a transmission.

Transceiver Design Considerations

Receivers will be connected in parallel as shown in Fig. 1. The coaxial line (RG 62) will be terminated at both ends. This line has a dc resistance of approximately 50 Ω/1000 ft. At 2000 ft the measured amplitude is approximately 55% of the input. For transmission over greater distances, a repeater device will be needed. The transceiver has been designed with the following considerations in mind.

1. DC isolated (minimize ground loops).
2. Common mode signal rejection.
3. Normal mode signal rejection.
4. Produce a minimum of line discontinuities.
5. Reliable response at maximum usable distance.
6. Be capable of driving the coaxial line and producing the required signals to meet the specifications.

The first two considerations are met by using transformer coupling. Normal mode signal rejection and reliable response at maximum usable distance is accomplished by building threshold limits into the receiver. See Fig. 4.

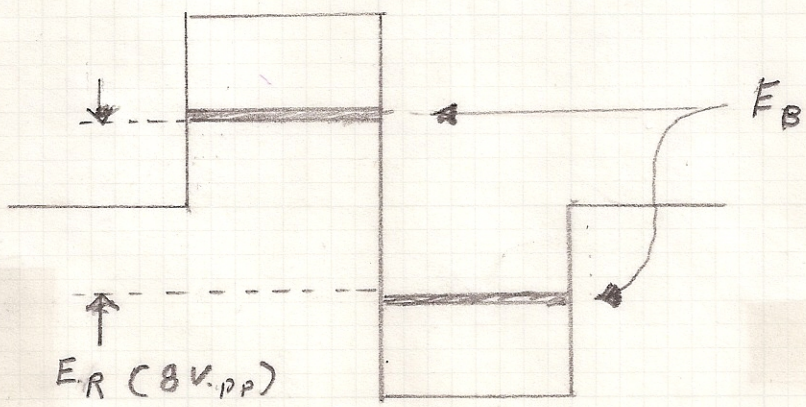

Figure 4 Typical Data Signal

E_R is a minimum level required for receiver operation. Below this level the receiver will not function. E_B defines an acceptance band of approximately 1 V. As long as normal mode noise on the line does not cause this acceptance band to be violated during the data signal, the receiver will operate properly. Actual tests with an rf source on the line indicate 8 V pp normal mode noise rejection. This threshold is fixed by the zener diode connected to the emitters of Q_1 and Q_2. The tests also indicate that the most sensitive frequency range is between 750 kHz to 2 MHz. The equivalent reflected capacity to the line is approximately 80 pF. This is isolated by a small resistance (approximately 40 Ω) so reflection from fast rise times are minimized. The dc reflected resistance is greater than 10 kΩ.

Receiver Operation - Figure 5

Normally Q_1 and Q_2 are both off. Q_1 is turned on by the negative phase of the signal. When they are turned on, the collector voltage changes from + 14 V to - 11 V. This causes the input pins 10 and 2 of 123A to change from + 5 V to 0. Figure 6 diagrams the receiver logic. Input 123A/9 serves as an enabling gate. The time constant (approximately 0.10 μsec) requires that a signal be present for at least 0.2 μsec before the 123A can be triggered. Once the gate is enabled, then a positive transition is required on 123A/10 to trigger the monostable. 123A/5 is the Q output. The negative phase of the frame pulse enables the 123A. 123A/5 and 123A/13 are respectively triggered by the logical zero out for the duration of the pulse width, approximately 1.3 μsec. 123E is triggered by either 123A/5 or 123A/13. This monostable serves as a delay (approximately 0.7 μsec) and drives the 13A chip. The 0.1 μsec signals on 13A/8 provide timing signals to drive the logic. The receiver registers are cleared by the pulse 08A/8 (see Fig. 5). Clock pulses used to shift the data through the receiver registers are produced at 00B/6. When another receiver on the line is replying its frame locks out all other receivers. This lockout pulse is produced by 00B/3.

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BY_____ DATE_____ SUBJECT REC. FIG. 5 SHEET No._____ OF_____

CHKD. BY_____ DATE_____ JOB No._____

DEPT. OR PROJECT_____

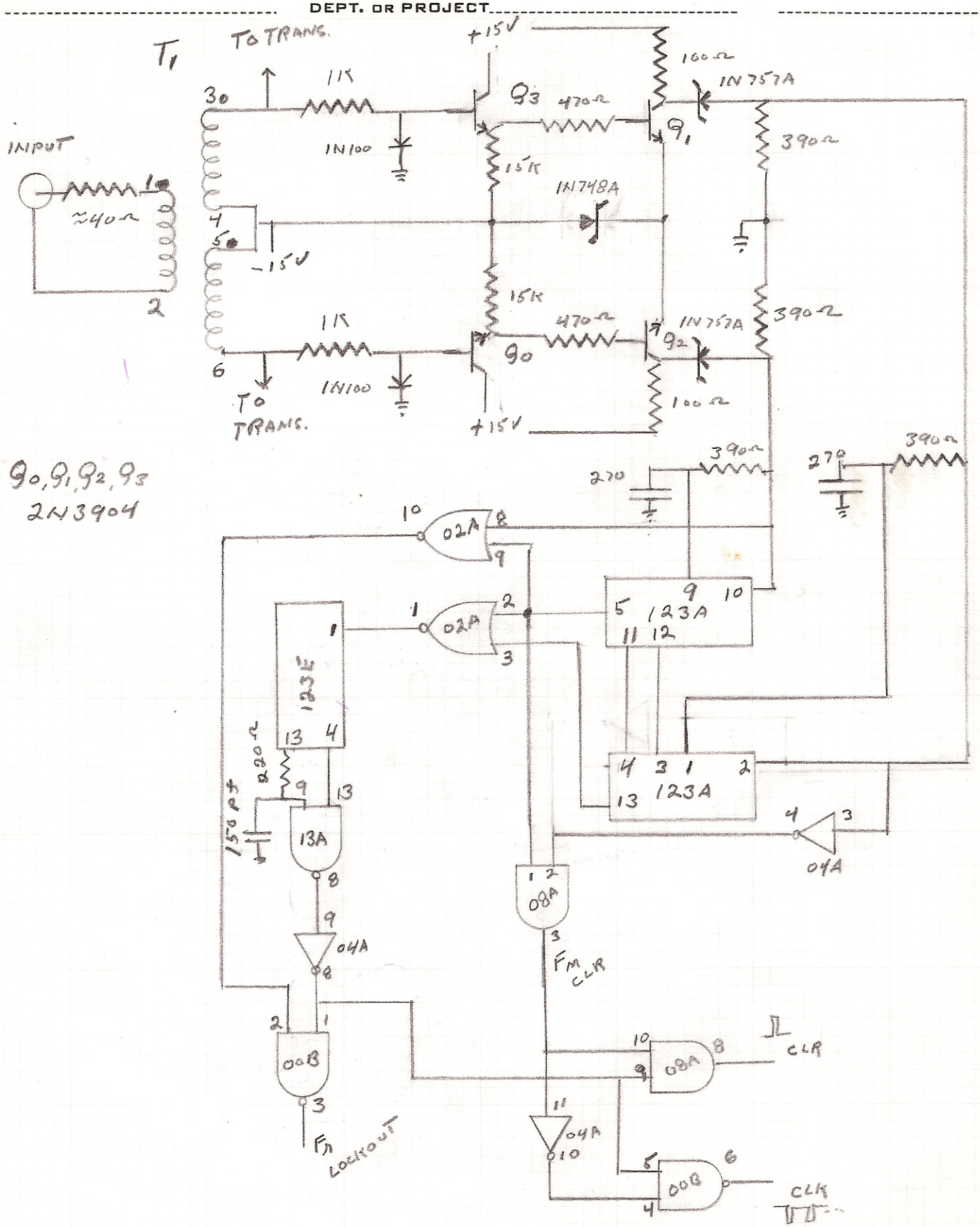
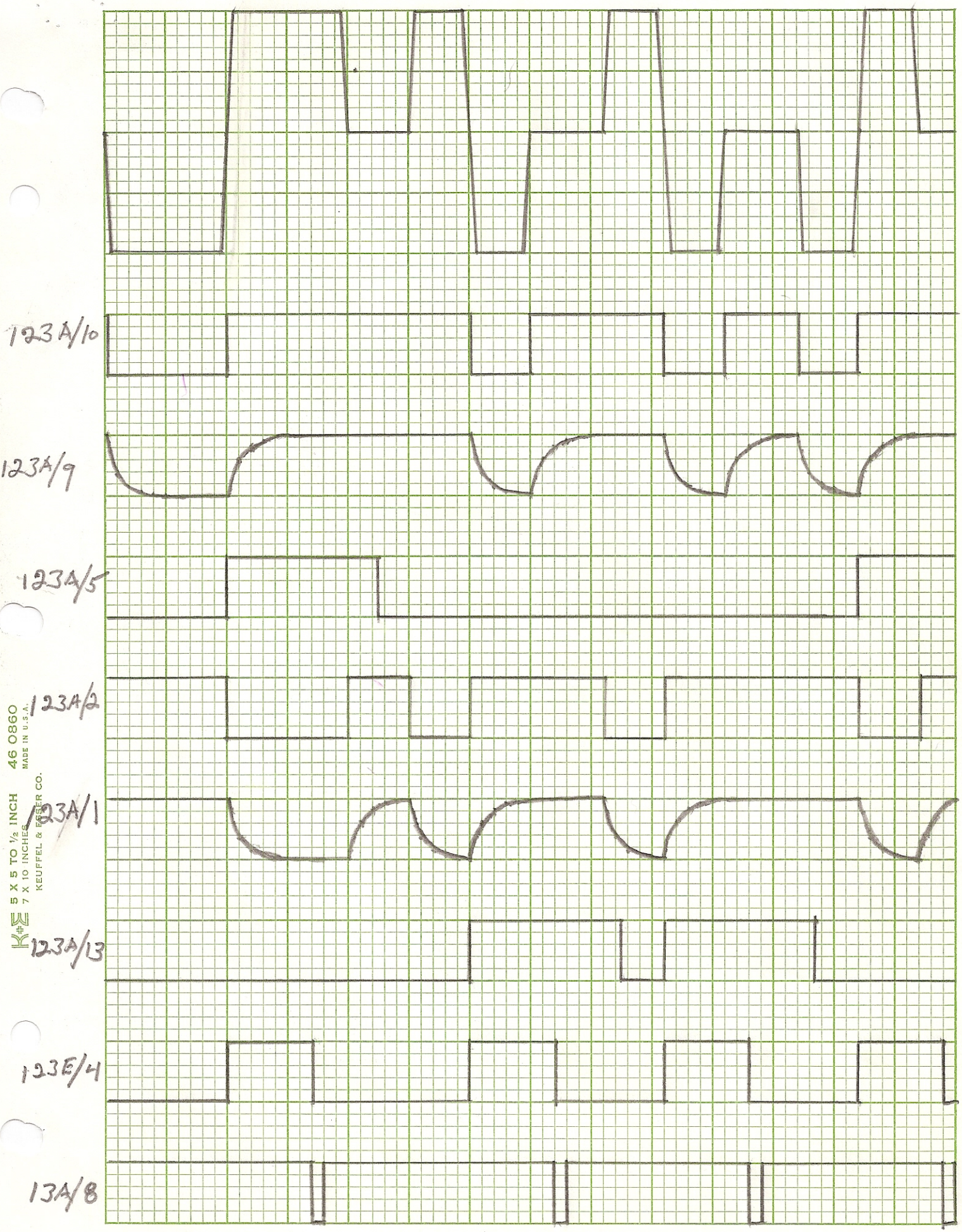


Figure 5.

SP 11037A



K+E 5 X 5 TO ½ INCH 7 X 10 INCHES KEUFFEL & ESSER CO. MADE IN U.S.A. 46 0860

Figure 6

Tolerances of logic widths: If the signal on the line meets the specifications, then the following tolerances are allowable in the logic.

123A/5 and 123A/13 = 1.3 μsec ± 16%
123E/4 = 0.70 μsec ± 21%
13A/8 ≤ 0.10 μsec.

Transmitter Operation

Q_4 and Q_6 (Fig. 7) serve as switches. Q_4 provides the positive phase of

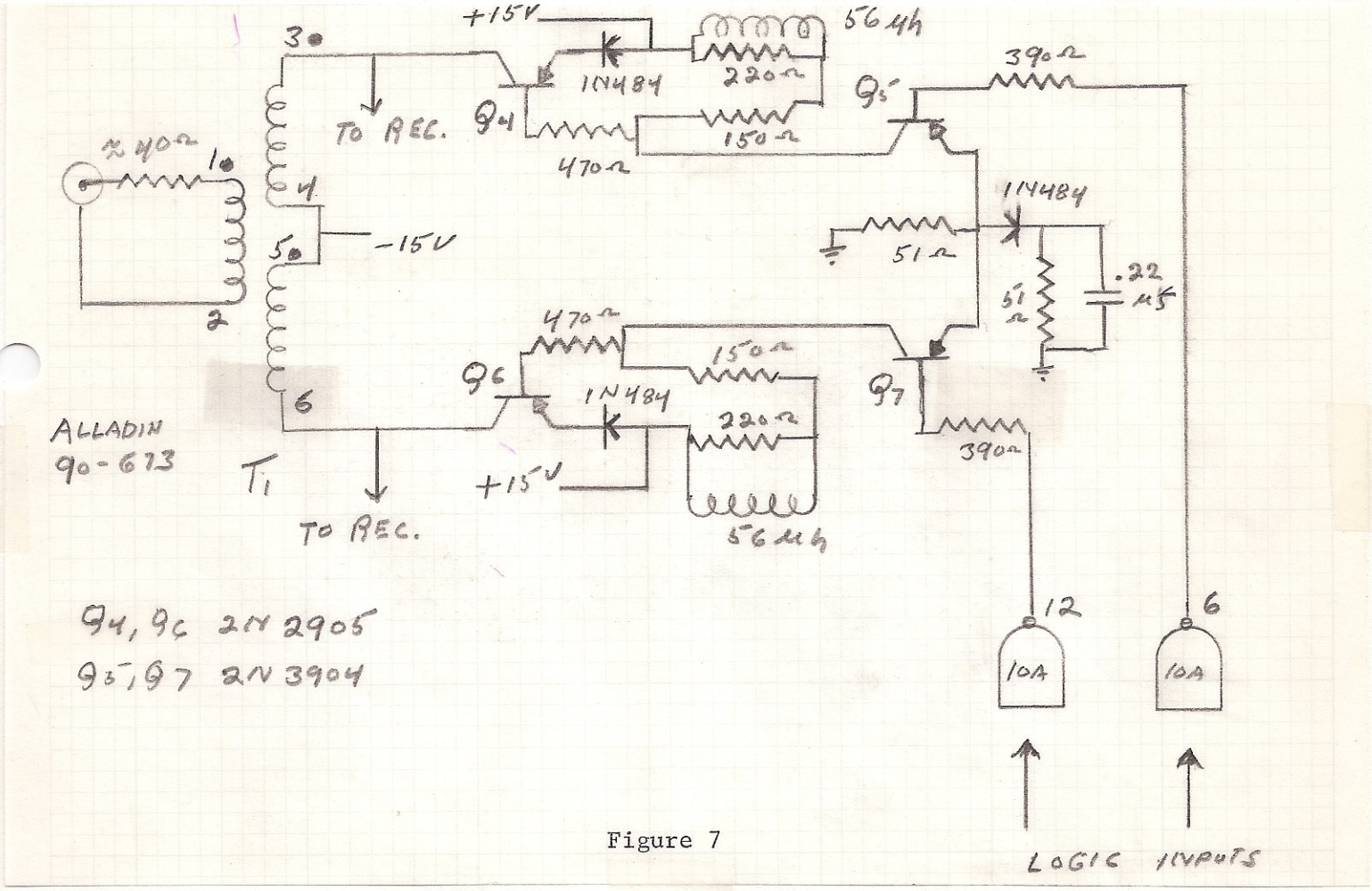


Figure 7

the signal and Q_6 provides the negative half. They are controlled by the logic inputs through the 10A chip. Approximately 60 V pp signals are produced across the output winding. Since the line is connected in parallel, the impedance that the output winding sees is approximately 46 Ω plus the 40 Ω output series resistor. The output resistor can be adjusted to meet the 30 V pp line specification.

Remarks, Tests and Results

The signal specifications are the result of a majority decision. It is obvious that for this particular transceiver the reliability could be improved by slightly altering the specifications. The reason for this is that the frame pulse is the only signal directly used to clear or lockout the transceiver. The data bits are derived from the 123A monostable. Its enabling gate requires a minimum signal width of 0.2 μsec. Once the 123A monostable is triggered, its output is independent of the input. By increasing the frame pulse width (10%), decreasing the data pulse width (10%), and altering the logic timing, a factor of two in timing tolerance could be gained.

Qualitative Tests on Common Mode and Normal Mode Signal Rejection

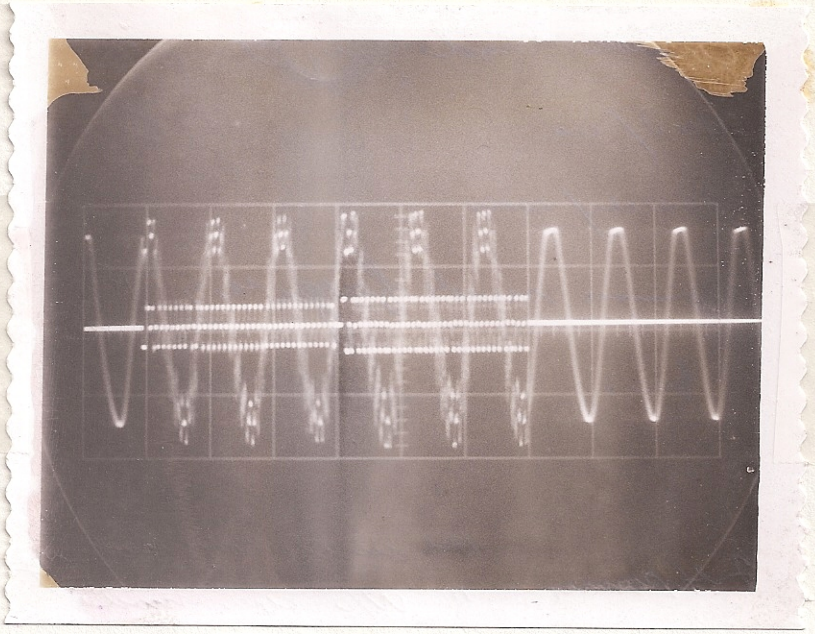
Common mode rejection tests were made in the frequency range of 20 Hz to 50 MHz. Picture 1 (40 V/cm 20 μsec/cm) is a double exposure. One exposure has a 50 kHz common mode signal added to the normal send/receive signal. For comparison, the common mode signal was turned off and a second exposure was taken. The normal mode to common mode ratio was measured as a function of frequency. The worst case (at approximately 1 MHz) is approximately 1/20. This indicates that about 160 V pp of common mode noise in the megacycle range will create enough normal mode signal (8 V pp) to disable the receiver.

Normal mode rejection was qualitatively studied in the same frequency range. The results (worst case) are shown in pictures 2 through 4. Picture 2A is a normal send/receive. Picture 2B is the frame and key signal. 3A and 3B (same respective amplitude and time base) show a normal component (8 V pp) added to the send/receive signals. The system still operates. In picture 4, the normal mode signal was increased to approximately 8.5 V. The transceiver was replying only about 10% of the time. The most sensitive frequency range is from 500 kHz to 2 MHz.

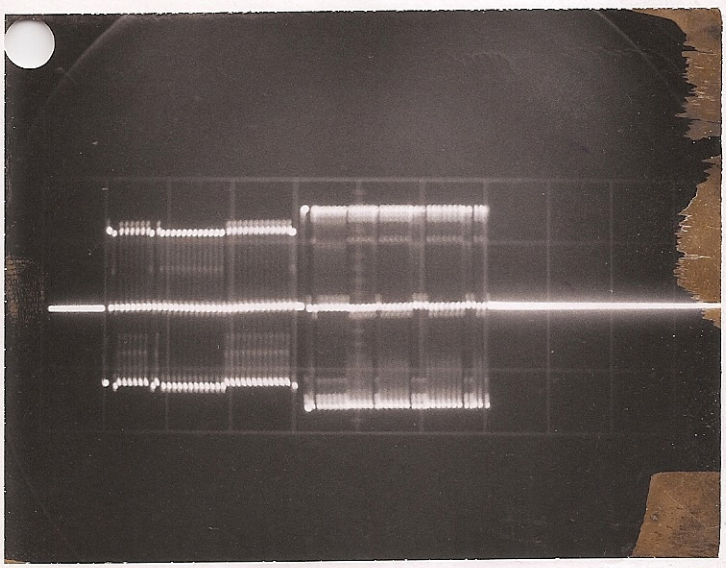
Other tests that were made on the transceiver indicate that:

1. It can stand a 50% mismatch in termination.
2. It will operate with a 10,000 pF cond. coupled through 30 Ω connected across the line.

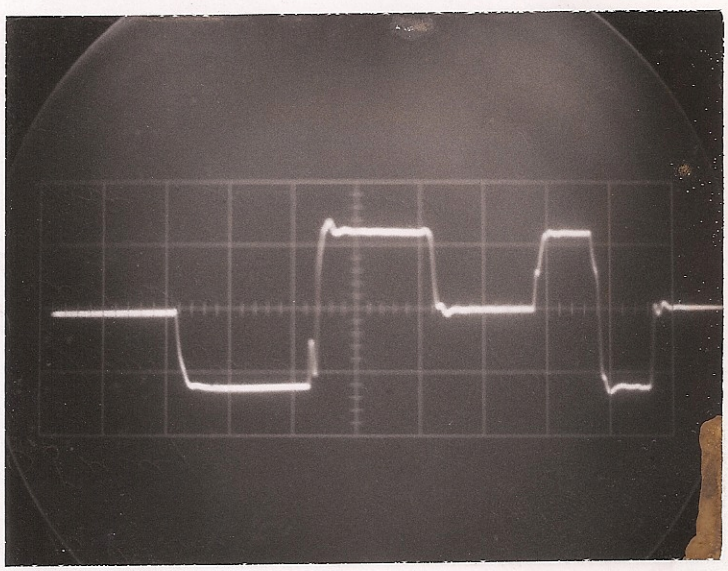
These last tests give some indication of how reliable the system will be when more units are added in parallel on the line.



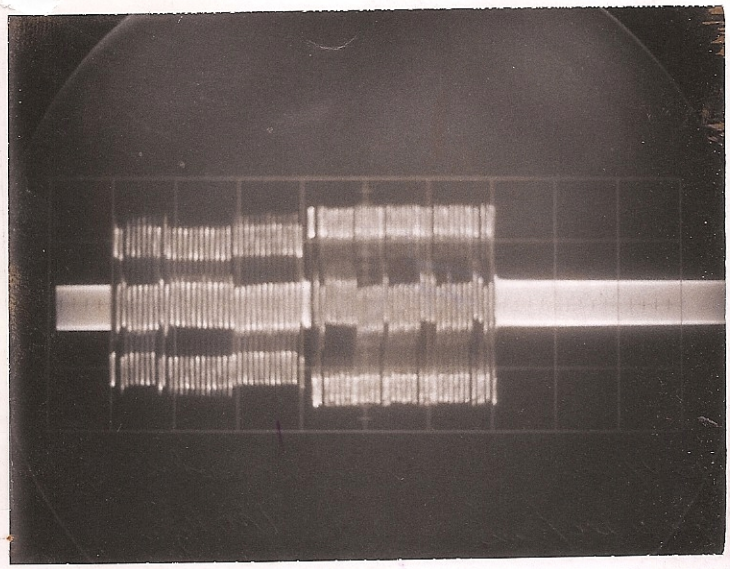
Picture 1. 40 V/cm
20 μsec/cm



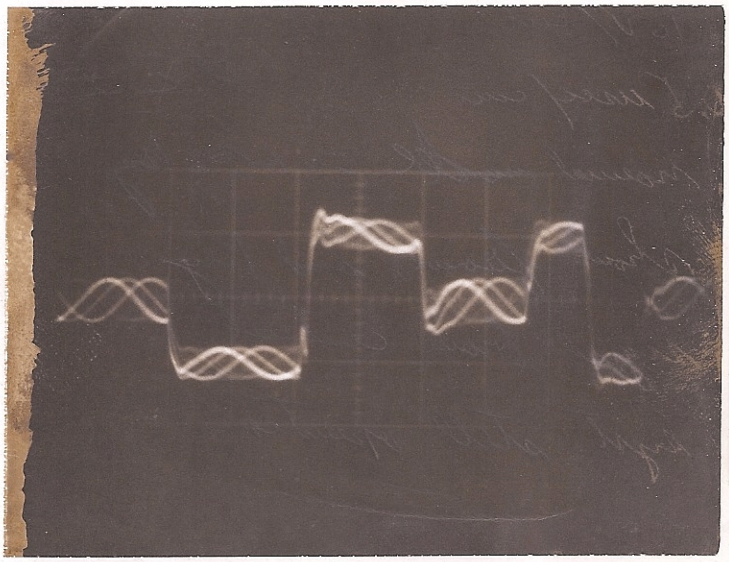
Picture 2A. 10 V/cm
20 μsec/cm



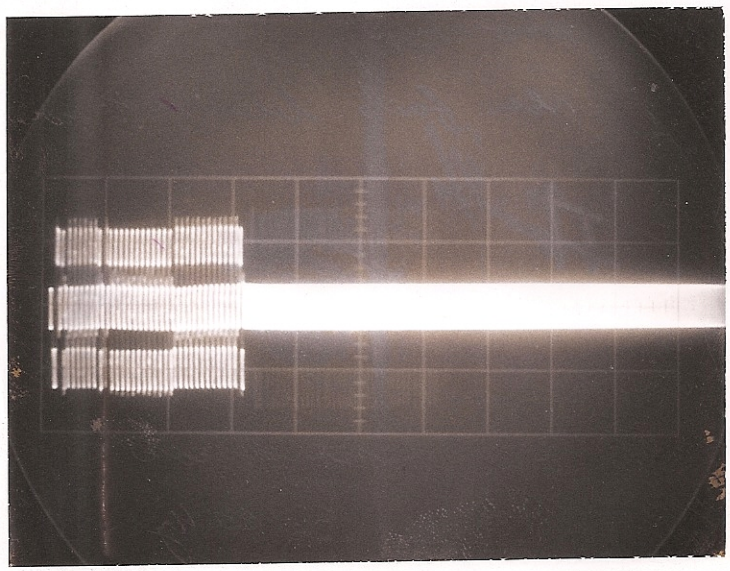
Picture 2B. 10 V/cm
0.5 μsec/cm



Picture 3A. 10 V/cm
20 μsec/cm



Picture 3B. 10 V/cm
0.5 μsec/cm



Picture 4. 10 V/cm
20 μsec/cm

VJK;ph
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