For Internal Distribution Only.

Alternating Gradient Synchrotron Department
BROOKHAVEN NATIONAL LABORATORY
Associated Universities, Inc.
Upton, New York 11973

Experimental Planning and Support Division Technical Note

. AGS/EP&S/Tech. Note 139.

C10 SEC PREAMPLIFIER

E. Beadle
January 21, 1992

Introduction

Resonant slow beam extraction (SEB) from the AGS requires precise control over the slope of the main magnet field intensity during the flattop portion of the AGS cycle. This is performed by the SEB Spill Servo System.[1] A component in the system is the C10 SEC preamplifier (D36-E164). The amplifier outputs a voltage directly proportional to the current produced by the beam intensity sensor (SEC or Ion Chamber) installed in the extraction line. The voltage is used by the spill servo system to control the main magnet fields in order to smooth the spill structure. This note summarizes the design, operation and specifications of the new preamplifier for the servo system.

The key performance parameters of the amplifier are summarized below:

TABLE I.

Gain (Ohms)	100 K - 2 Gig (1,2,10 sequence)
Output Voltage	3 V into 50 ohms (nominal)
Gain Accuracy	Better than 10% @ 25°C
DC Offset	< 20 mV @ 25°C
RMS Noise	< 100 mV (BW = 15KHz, Gain = 2×10^9)
3 db Bandwidth	> 2.5 KHz (@ input capacitance < 5 nF)
Packaging	Single width NIM (Other options available)

1.0 Approach.

A block diagram of the amplifier is shown in Fig. 1. The amplifier input current is generated by a beam intensity monitor which is an ideal current source. The monitor output current is directly proportional to the extracted beam intensity as a function of time. Because both high gain-bandwidth product and large dynamic range are required, the amplifier front end is a two stage cascade of variable gain amplifiers.

The gain is set either using a rear panel "D" connector or by the front panel dip switches. Programming the gain through the rear panel requires four TTL lines. The front panel dip switches are priority encoded to resolve conflicts when two or more switches are pressed by setting the highest gain selected. The table below displays the programming required to select each gain.

Amplifier Gain Selection Table.

GAIN	7 SEG DISPLAY	Gain Bits H/L	2	1	0	HI/LO SW	DIP SW "ON"
100K	0	0	0	0	0	LO	0
200K	1	0	0	0	1	LO	1
1M	0	1	0	0	0	HI	0
2M	1	1	0	0	1	HI	1
10M	2	1	0	1	0	HI	2
20M	3	1	0	1	1	HI	3
100M	4	1	1	0	0	HI	4
200M	5	1	1	0	1	HI	5
1G	6	1	1	1	0	HI	6
2G	7	1	1	1	1	HI	7

H/L = HI/LO control input.

C10 PREAMP BLOCK DIAGRAM

ERB 1/17/91

(GAIN CONTROL NOT SHOWN)

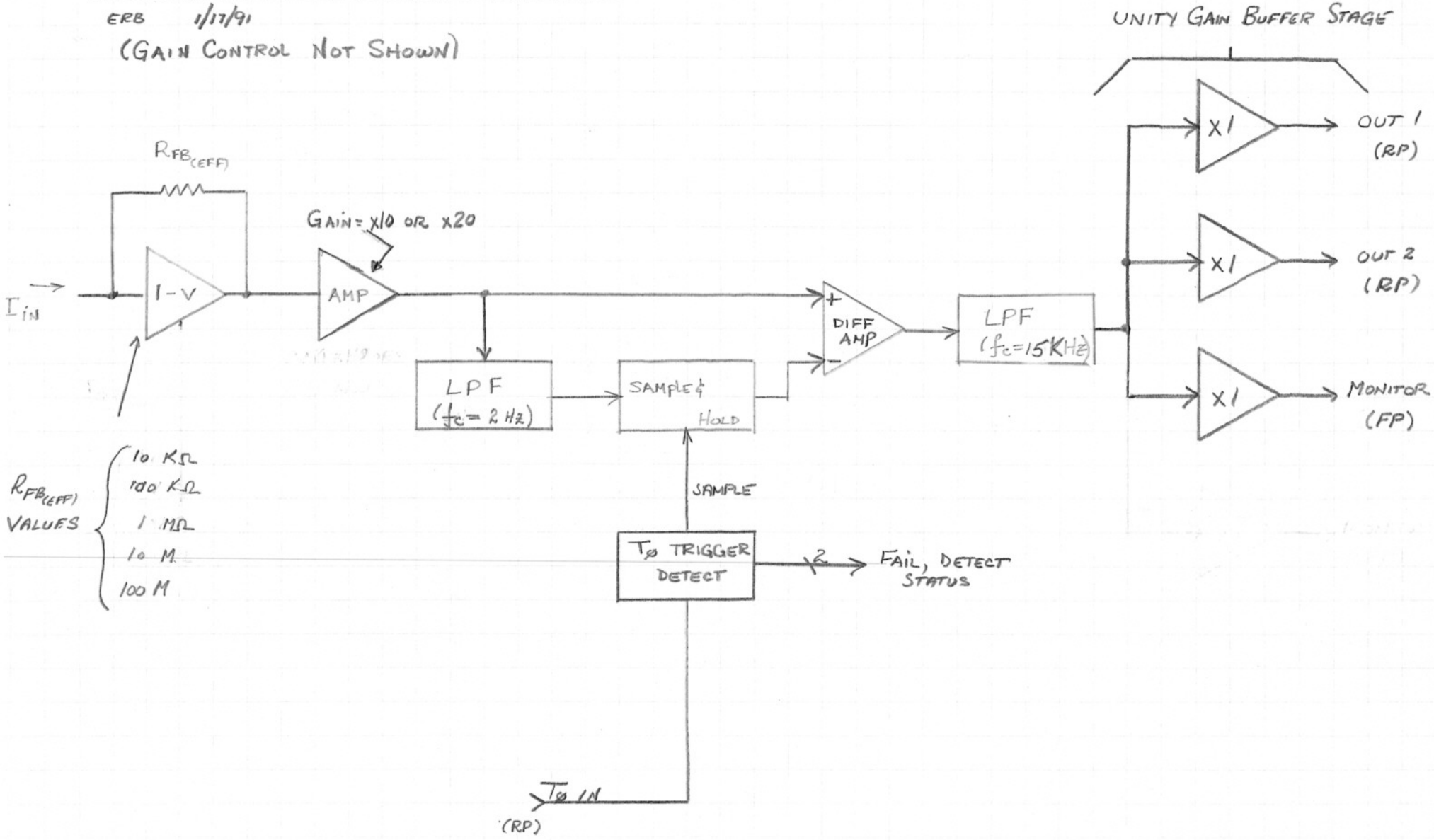

FIGURE 1

Because the circuit has high gain, standard techniques for offset correction using nulling pots will not be effective. This is because the temperature coefficients are multiplied by the high circuit gain. Also, drift due to circuit aging will also cause the offset value to change dramatically due to the amplifier gain. Therefore, correction of the DC offset is performed using a sample/hold and subtractor in an auto-zeroing circuit. The offset is sampled in each AGS cycle during a 60 ms (nominal) window triggered by each T_0 pulse. During this window theamplifier output can exceed $\pm$ 200 mV before acquiring the offset. In this way the initial DC offset and any drift in the offset are zeroed on each pulse. An R-C low pass filter attenuates the circuit noise that would corrupt the sampled value of the offset. The sampled value is held for the entire AGS cycle and is subtracted from the front end output. After extraction is complete the low pass filter requires 375 ms to reacquire the offset to within 1%.

The output stage of the circuit includes a low pass filter and a fanout/buffer stage. The filter limits the noise bandwidth of the amplifier alone to approximately 15 KHz (neglecting cable capacitances). The output signal is fanned out and buffered to drive two independent rear panel outputs and one front panel output. The typical drive capability of each output is 10 V (dc peak) into 50 ohms. Each output is independently buffered, short circuit protected, and available on isolated BNCs with the capability to jumper the shield to the board ground. The jumpers are located internal to the module. These jumpers are intended primarily for ground loop isolation testing. No other ground path is provided.

Digital outputs and front panel LEDs have been included as diagnostics. The outputs include LOCAL/COMPUTER readback and T_0 detection monitoring. The LOCAL/COMPUTER readback is active-hi for LOCAL mode. An LED on the front panel indicates the selection. LOCAL mode is indicated by the LED being "on."To switch the module between LOCAL and COMPUTER control, the front panel LOCAL/COMPUTER switch is used. For T_0, each time a pulse arrives, the front panel T_0-Detect LED flashes for approximately .1 second. However, if the time between T_0 pulses exceeds approximately 10-12 s the T_0 FAIL flag is activated and the T_0 FAIL front panel LED is lit. This indicates that T_0 has not been received for at least 10 s, the flag is reset automatically when the next T_0 pulse arrives. The T_0 detection circuit is insensitive to the duty cycle and period of the T_0 pulse train. Additionally, the detection circuit has been designed with thresholds for minimum pulse width and amplitude. This minimizes the probability of triggering the circuit due to transients or noise.

2.0 Circuit Design.

2.1 Front Current to Voltage (I-V) Converter.

The first stage of the amplifier is a current to voltage converter. In order to maintain an acceptable noise floor with the required gain and bandwidth, the circuit is configured with a resistive "T" feedback network. The "T" configuration has been optimized to balance DC offset, I-V gain, noise, bandwidth and parasitic effects. The front end amp provides gain ranging from 10 K to 100 Meg in decade steps. Gain switching is accomplished using relays, because at the time the circuit was designed, semiconductor switches had leakage currents larger than the currents to be measured. Through experimentation on the bench it was found that the highest gain settings must be selected by the normally closed relay states. This is because there is detectable leakage current from the coil to contacts.

The input impedance of the modules is 5.1 K. This value was selected because it is largest value that can be used without degrading the circuit bandwidth, due to input capacitance caused by cable loading, while minimizing the voltage gain for pick-up signals. To further reduce noise pickup, an inductor is used in series with the 5.1 K resistor. It was found during field tests that protection diodes across the input amplifier were necessary to prevent the first stage opamp from failing.

The resistor type chosen for this and the following stages are CADDOCK metal film with .1% accuracy and a 25 ppm/deg C tempco. Metal film resistors were chosen because of the superior noise performance as compared to carbon composition types. The high precision and low tempco is selected to keep the initial gain accurate and maintain accuracy over the temperature range of 0 - 40^{0}C. The CADDOCK resistors were chosen because they are available in CK06 cases and thus are easy to place on a board.

The opamp selected is an OP42 because of its low bias current, low current noise and AC performance. To further minimize noise inherent in the opamp the supply rails for the front end amplifier are regulated to 12 V. It was found that the front end noise was reduced when operating from 12 V rails. In this application operating at $\pm$ 12 V rails does not adversely effect the opamp performance or limit the circuit performance.

2.2 Offset Nulling Circuit.

A sample and hold approach for removing the front end DC offset to restore the input signal baseline is used in the module. The baseline is restored by subtracting the front end output from the held value of the offset. A pulse discriminator circuit, comprised mainly of two one-shots and comparator, is included in the S/H trigger hardware and prevents random noise from triggering an acquisition cycle. The offset is acquired to .01% within 60 ms and is held with a droop rate of < .05 mv/sec. For other applications the hold capacitor can be reduced to .01 uF to reduce the acquisition time to .5 ms for .01% acquisition; however, the droop rate will increase to 5 mv/sec.

To eliminate circuit and pick-up noise from corrupting the DC sample, the front end gain output is "integrated: by an R-C los pass filter. This attenuates the noise leaving only the DC offset. However, the filter will pass the input pulses and elongate their tails. Therefore, before sampling the offset for the exit AGS cycle, the delay time between the end of extraction and the next sample epoch should be at least 375 ms (5 time constants).

The AD582KD was selected because it provides sufficient performance and is a stock part. The circuit is used as a noninverting gain of 1 but can be modified for other gains > 1. The opamp stage following the sample/hold circuit subtracts the offset from signal plus offset. A low leakage capacity such as mylar film is used as the hold capacitor because the sample value must be held for several seconds.

2.3 Output Buffer.

The output buffer and filter is used to attenuate the wideband noise generated in the amplifier and boost the output drive capability of the module. The module supplies a total of four outputs, each with a typical drive capability of 10 V (dc peak) into 50 ohms. To boost the current drive and maintain the circuit performance a current buffer is used in the feedback loop of an opamp. The opamp selected is the OP470 because it has four amplifiers in a package. In addition to increased current drive, the output stage is short circuit protected. Input resistors on the opamp and current buffers limit the input currents and prevent damage to the ICs in overload conditions. The Elantec EL2003 current buffers provide automatic shutdown on thermal and short circuit overloads. The required heat sinking has been provided.

2.4 Control Hardware.

The control hardware is used for monitoring the amplifier and setting the gain. The control hardware functions consists of:

a) Local/Computer Mode Switching
b) Gain Programming
c) Loss of T_0 Pulse Detection.

To set the LOCAL or COMPUTER mode, a front panel switch is used. Int the LOCAL mode the front panel readback LED will light and the rear panel LOCAL/COMPUTER readback line will assume a TTL hi output. In the COMPUTER mode the readback line assumes lo and the LED is off. Gain programming is performed in either the LOCAL or COMPUTER modes. In the LOCAL mode the front panel dip switches are used. The user selects one of the gain settings by pressing one of the front panel dip switches. The selection is decoded and multiplexed to the relay driver circuits (2N2905 transistors) and to the front panel 7 segment display. For gain control in the COMPUTER mode, an external source must provide 4 TTL bits to the module. The bits must be held by the external source.

Also, the presence of T_0 is monitored because loss of T_0 means that the DC offset circuitry is not continually triggered. To detect the loss of T_0 a retriggerable oneshot (74LS123) is used as a timer to detect when the period has exceeded the limit of 10-12 s. Another pair of 123s and a comparator act as a pulse height and width discriminator. The discriminator provides a safety margin against noise spikes triggering the T_0 sample strobe.

---

[1] AGS Tech. Note 147, A. Soukas, et al.