BNL USE ONLY

Accelerator Department
BROOKHAVEN NATIONAL LABORATORY
Associated Universities, Inc.
Upton, New York 11973

EP&S Division Technical Note No. 102.

G. Benenson
June 30, 1983

DATACON/Q-BUS INTERFACE BASED ON DRV11-P

I. General Description

The amount of monitoring and control function required for successful operation of the AGS is growing rapidly, and already exceeds the capability of the existing mainframe computer/communications system. The obvious solution is to move some of the problem to dedicated, distributed front-end microcomputers. Availability of peripherals and broad familiarity with its programming languages make the DEC LSI-11 series a logical choice for the front-end machine. A major barrier to systems integration of distributed computers has been the lack of interfacing hardware for connecting to the existing DATACON II network. This note describes an interface which connects the LSI-11 Q-BUS to a DATACON crate controller via a DATACON-RS422 converter card (D09-E1328). To DATACON, the interface makes the LSI-11 system appear as a remote receiver; to the LSI-11, it makes DATACON a standard peripheral, occupying 4 I/O addresses, and accessible under program or interrupt control.

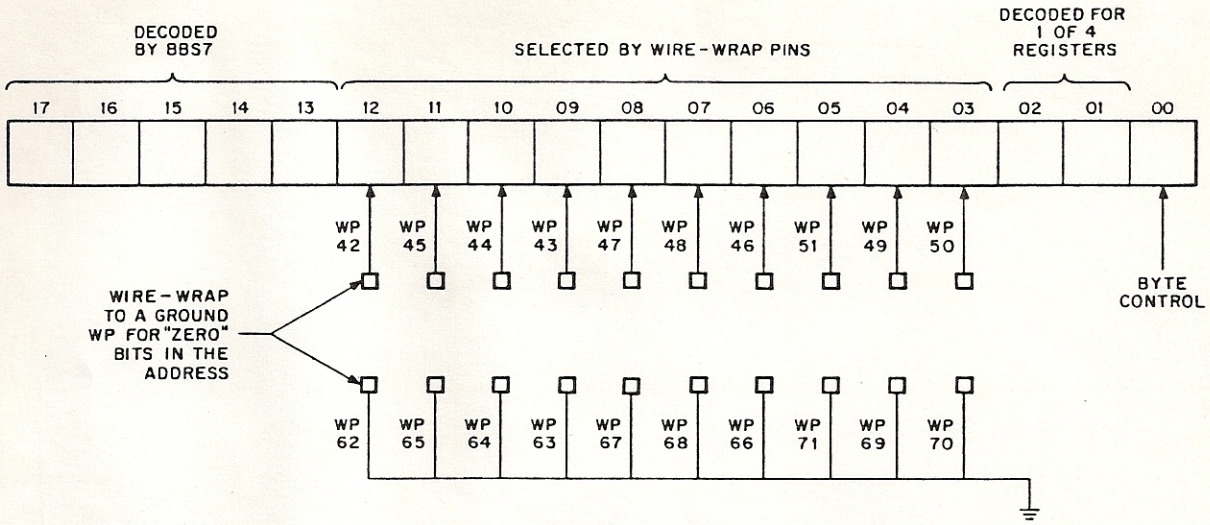
The interface is based on the DEC quad-sized DRV 11-P foundation module,[1] which includes address decoding, bus transceivers and protocol logic and interrupt logic. The remaining circuitry is implemented on the user I.C. section of the card. The module communicates via 40-conductor ribbon cable with the DATACON RS-422 converter. Signals are driven and received differentially by standard RS-422 interface chips, and either flat or twisted-pair cable may be used, according to length-of-run and environment.

II. User's Guide

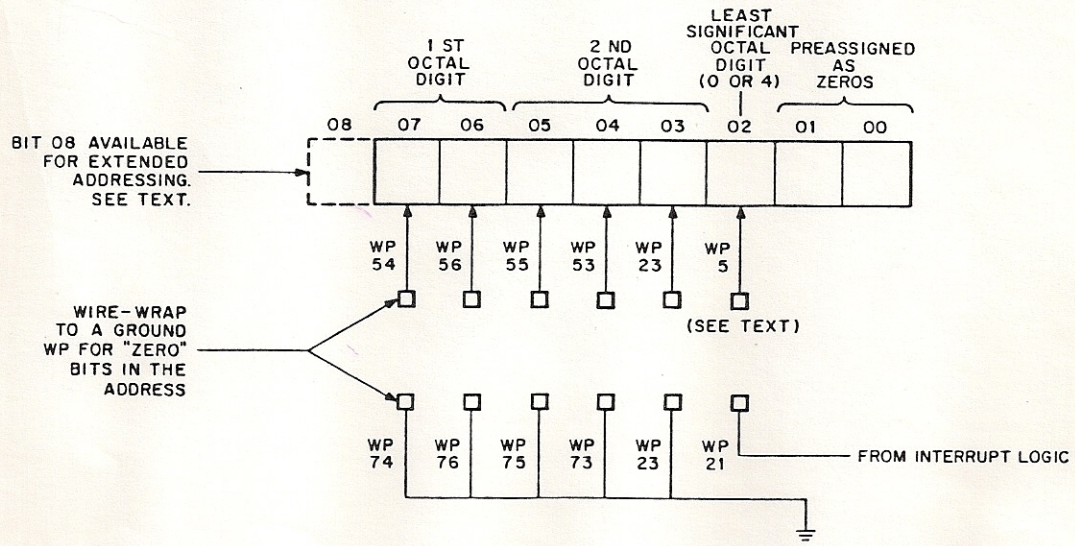
Q-BUS address of the interface is selected using wire-wrap jumpers, as shown in Fig. 1. The four register locations are shown in Table 1. At the end of a 32-bit transmission from DATACON (via RS-422 card and

DRV11-P DATACON / Q-BUS INTERFACE

REGISTER ADDRESS SELECTION



INTERRUPT VECTOR ADDRESS SELECTION



INTERRUPT VECTOR FORMAT

7 6 5 4 3 2 1 0

*	*	*	*	*	1	0	0

SET INTERRUPT (ACCEPT DATA)

*	*	*	*	*	0	0	0

READ INTERRUPT (TRIGGER REPLY)

* SELECT USING WIREWRAP JUMPERS, AS SHOWN.

FIGURE 1

DRV 11-P DATACON / Q-BUS INTERFACE

REGISTER CONFIGURATION

ADDRESS	DESCRIPTION	TYPE	CONTENT
7{7/6}xxx0	INPUT DATA BUFFER REGISTER (IDBR)	READ ONLY	MAGNITUDE
7{7/6}xxx2	CONTROL/STATUS REGISTER (CSR)	(SEE BELOW)	
7{7/6}xxx4	OUTPUT DATA BUFFER REGISTER (ODBR)	READ/WRITE	MAGNITUDE
7{7/6}xxx6		READ/WRITE	STATUS

CONTROL/STATUS REGISTER (CSR) FORMAT

BIT	NAME	TYPE	DESCRIPTION
15	$\overline{\text{SET}}$/READ	READ	INPUT DATA FROM DATACON
14 ↓ 8	COMMAND (7)	READ	
7	READY	READ	SET BY DATACON ACCEPT; RESET BY INIT, RESET OR LD6
6	INTERRUPT ENABLE	READ/WRITE	ENABLES INTERRUPT ON READY
5	ERROR	READ	SET AFTER 200μS DURATION OF READY; RESET BY INIT OR RESET
4	DONE	READ	SET AFTER COMPLETED RESPONSE TO DATACON; RESET BY INIT, RESET OR READY.
3 ↓ 1	(NOT USED)		
0	RESET	WRITE	CAUSES RESET OF READY, ERROR & DONE

TABLE I.

ribbon cable), the 16-bit magnitude field will reside in the Input Data Buffer Register; and the 7-bit command field plus set/read bit will be stored in the high order byte of the Control/Status Register (CSR).[2,3] In addition, the CSR READY bit will be set to indicate receipt of a transmission. (See Fig. 2.) If the INTERRUPT-ENABLE bit has been set by the processor, the READY bit will also trigger an INTERRUPT. Two vectors are used: one for SET operations; the other for READS. Interrupt vector addresses are also selected by the wire-wrap jumpers; see Fig. 1.

If INTERRUPTS are enabled, the CPU should respond to the incoming DATACON transmission during the service routine; otherwise, polling of the READY bit must be used. In either case, the processor is required to respond within 200 µsec. Lack of response will cause the CSR ERROR bit to be set. Further transfers in either direction will be inhibited until the ERROR bit has been cleared by Q-BUS INIT, or by writing to the CSR software RESET bit. A race condition could potentially occur if the 200 µsec timeout and a late response from the CPU were to occur simultaneously. However, the interface avoids this situation by using look-ahead circuitry to detect an ERROR before initiating the REPLY to DATACON. As a result, setting of the ERROR bit and completion of the DATACON cycle are mutually exclusive.

A valid CPU response to a DATACON transmission is accomplished by writing to the two output data buffer register (ODBR) locations (Table I) in increasing order of address. Transfer of the second word actually triggers the REPLY bit to DATACON. The data bits are then shifted out under control of DATACON. A DONE bit in the CSR is set at the end of the transfer; the DONE bit will be reset by the next READY. For diagnostic purposes, the two ODBR registers may be read as well as written. Because they are wired as a recirculating 32-bit shift register, the original data is preserved at the end of a response cycle.

III. Circuit Description

Interface schematics are shown on Dwg. # DO9-E1498-3, Sheets 1 and 2 of 2. For simplicity, these will be referred to as p.1 and p.2 respectively.

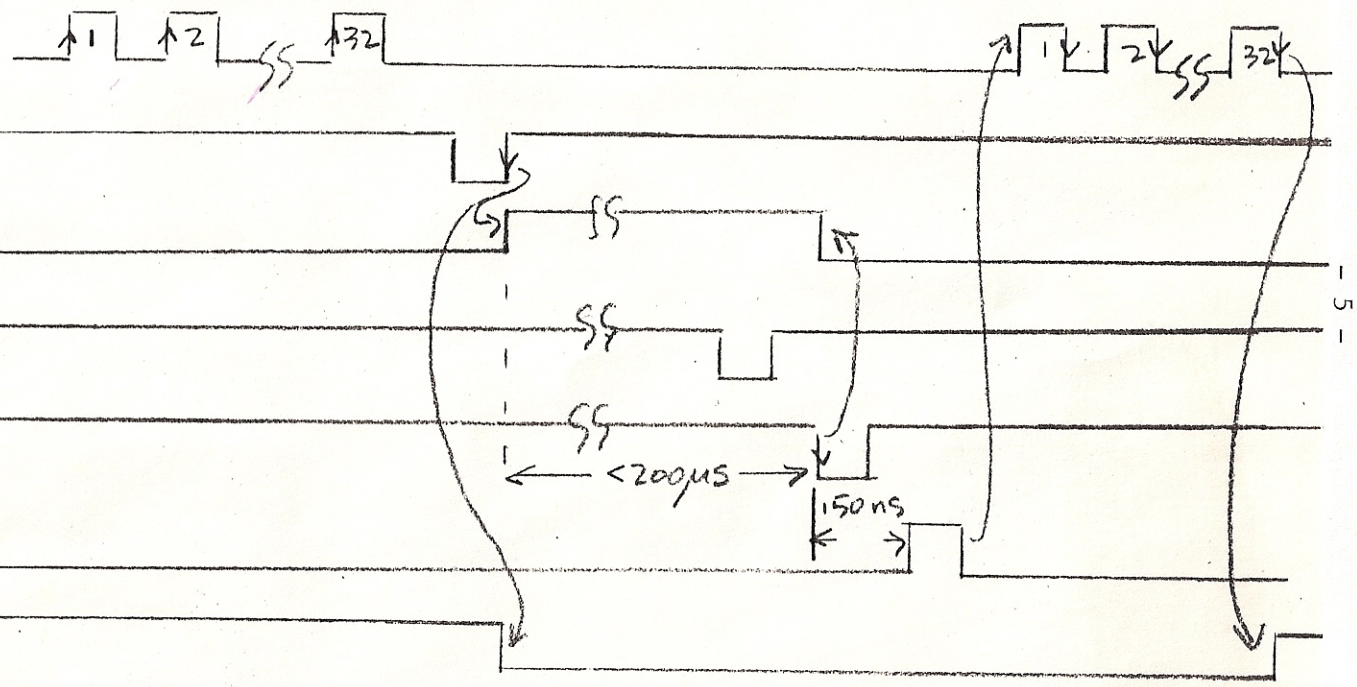
Incoming RS-422 pairs from DATACON are received by U15 (p.1). The CLOCK and DATA lines are fed directly to the clock and serial data input of a 23-bit shift register composed of H43, H31 and H19 (p.2). H19 and H31 are read to Q-BUS at the IDBR location; H43 contains most of the upper byte of the CSR (command field). Once the incoming transmission has been com-pleted, DATACON sends a 1 µs wide ACCEPT pulse. The trailing edge of AC-CEPT clocks register P24, which stores INTERRUPT requests, READY and the SET/READ bit.

Register addresses 0, 2, 4, and 6 are assigned to the IDBR, CSR and 2 ODBRs, respectively. (See Table I.) DATO to a register produced a LD

DRV11-P DATACON / Q-BUS INTERFACE

TIMING SEQUENCE FOR MAIN HANDSHAKE

SIGNAL NAME	SIGNAL SOURCE	PIN LOCATION *
CLOCK	DATACON	U15-11
$\overline{\text{ACCEPT}}$	DATACON	U15-3
READY	CSR7	P24-10
$\overline{\text{LD4}}$	Q BUS ($\overline{\text{DATO}}$ · SEL4)	H55-6
$\overline{\text{LD6}}$	Q·BUS ($\overline{\text{DATO}}$ · SEL6)	H55-3
REPLY	ONE-SHOT	BB 24-5
DONE	CSR4	P14-13



(NOT DRAWN TO SCALE)

* REF:
D09 E1498-3
SHEET 1/2

FIGURE 2

pulse with the appropriate subscript (see P.1); DATI from an addressable register produces RD. For example, reading of the CSR is enabled by RD_2, etc. Registers 0, 4 and 6 and the high-order byte of 2 are read via a tri-state bus wired to the IN lines of DRV 11-P; the low byte of the CSR uses the $SPARE_{7-0}$ lines and is enabled by the 2 SPARE ENB bits.

One the READY bit has been set, the processor is expected to produce LD_4, followed by the LD_6, within 200 µs. If it arrives before the end of the timeout, LD_6 resets READY and triggers the 1 µsec REPLY to DATACON. Should the trailing edge of the timeout (M24-4) find READY still on, the ERROR bit (K19.5) will be set. The potential race condition is avoided by deferring REPLY (BB24-5) until after a 150 ns wait (BB24-4) to cover propagation delays in recognizing an ERROR condition. If the ERROR bit has been set, it will inhibit the REPLY even though LD_6 occurred also.

The response part of the cycle is initiated by the REPLY bit. Following transmission and propagation delays, DATACON issues a stream of 32 pulses on its CLOCK line. The interface is expected to shift its output data bit serially in synchrony with the trailing edges of these clocks. Serial data from the interface appears in parallel on the DATA I and DATA II lines; together with REPLY, these lines are buffered by RS-422 drivers, BB14.

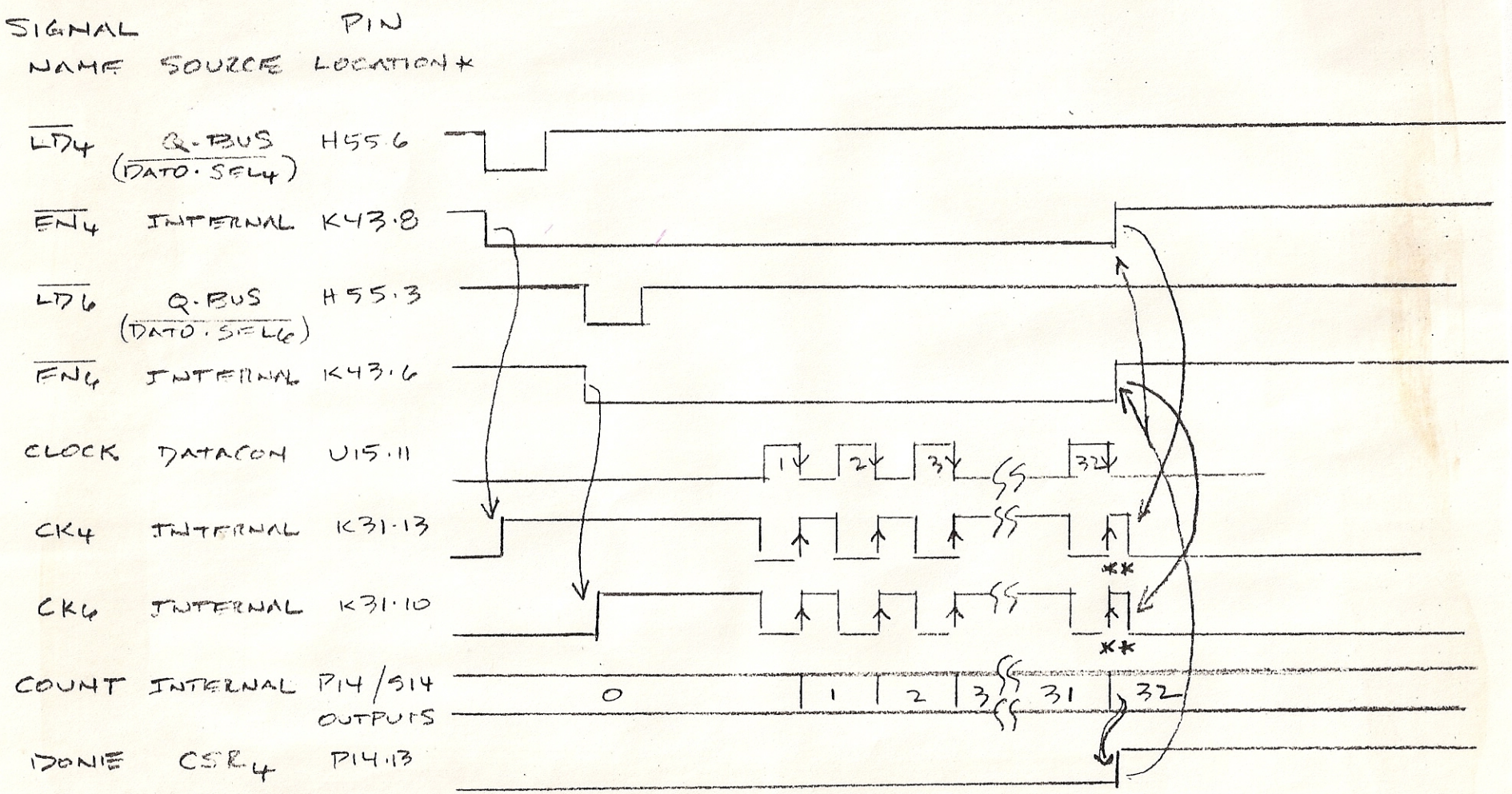
The output data buffer consists of 74199 shift register chips A11, A25, A39 and A53. These devices are parallel-loaded from Q-BUS via tri-state buffers C19, C25, C39 and C53. Because the 74199s are both loaded and shifted sychronously, a total of 33 clocks must be provided to complete the sequence: the first for loading and the remainder for shifting. At the end of this cycle, the DONE bit is produced in the CSR. The circuitry for controlling the ODBR and DONE bit consists of 32-bit counter S14 and P14, clock-enable flip-flops K43 and miscellaneous combinational logic (P.1). Because the two LOAD pulses LD4 and LD6 do not coincide, neither can the respective clock pulses CK4 and CK6. Therefore, there are two enable lines, each set by its respective LD line, and reset after 33 clock edges, by DONE (see Fig. 3).

III. Conclusion

Interfacing of Q-BUS to DATACON has proven relatively simple. The required interface card consists of a DEC DRV11-P with 31 ICs added to the user wire-wrap section, and a small number of discrete components. Total component cost is approximately $300, and about 600 wire-wrap wires must be installed.

DRV11-P DATACON/Q-BUS INTERFACE

TIMING SEQUENCE FOR OUTPUT SHIFT REGISTER & DONE BIT



* REF: D09E1498-3 1/2

** NOTE: WIDTH OF THIS FINAL CLOCK PULSE IS DUE ENTIRELY TO PROPAGATION DELAYS

FIGURE 3

REFERENCES

1. Microcomputer Interfaces Handbook, Digital Equipment Corp., 1981, pp. 310-334.

2. B.B. Culwick and R. Frankel, "DATACON 2 64-Channel Remote Receiver", CHAOS Hardware Note D2RRA, AGS, June 1974.

3. B.B. Culwick, "DATACON 2 Transmission Bit Definitions and Terminology", AGS Computer Note #31, July 1973.