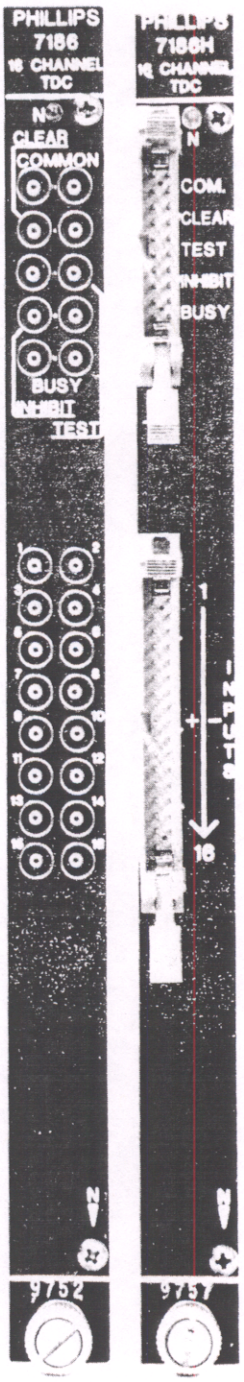
Phillips Scientific

16 Channel Time to Digital Converter

CAMAC MODEL 7186 7186H



FEATURES

* Model 7186 features NIM Inputs with Lemo Connectors
* Model 7186H features Differential ECL Inputs
* 7.8 μSec Conversion and Processing Time
* 12-Bit Dynamic Range, Resolution down to 25 pSec/Count
* Programmable Pedestal Correction
* Sparse Data Scan with Lower and Upper Time Cuts
* Fast Clear and Inhibit
* COMMON START or COMMON STOP
* Built-in Test Features check TAC and Digitization

DESCRIPTION

The Model 7186/H TDC implements 16 channels of Time to Amplitude Conversion (TAC) followed by a digital processing section and CAMAC interface in a single width CAMAC module. To minimize data readout time, the module performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following the COMMON input. It may be delayed by a user-programmable amount to allow time for derivation of FAST CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel FAST CLEAR or CAMAC commands.

Several user selectable time ranges are provided:

Range	Resolution		Range	Resolution
100 nSec	25 pSec		1 μSec	.25 nSec
200 nSec	50 pSec	OR	2 μSec	.50 nSec
400 nSec	100 pSec		4 μSec	1.0 nSec
800 nSec	200 pSec		8 μSec	2.0 nSec

Note: All channels need not have the same scale factors. Custom ranges are available when ordering.

INDIVIDUAL START or STOP INPUTS

7186 : Fast negative NIM, direct coupled bridging input (1 KΩ impedance); user must terminate end of daisy chain with 50 Ω; minimum pulse width 10 nSec.

7186H : 100 Ω, differential ECL, 100 mV threshold. Minimum input pulse width 10 nSec.

COMMON CONTROL SIGNALS (COMMON, CLEAR, INHIBIT, TEST)

7186 : Two bridged Lemo inputs to facilitate daisy chaining (1 KΩ impedance).

7186H : Two pairs of differential ECL inputs to facilitate daisy chaining (1 KΩ impedance).

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150 Hilltop Road • Ramsey, NJ 07446 • (201) 934-8015 • Fax (201) 934-8269

Digitization Time : 7.8 μsec minimum, includes 1 μsec for settling and for accepting Fast Clear signals prior to digitization. Timing is measured from the leading edge of the COMMON signal. Digitization may be delayed by 0 to 16 μSec in 62.5 nsec increments with external jumpers. An increased delay is mandatory in COMMON START mode and may be used in either mode to allow a greater acceptance window for Fast Clear signals. For ranges $\leq$ 800 nsec full scale, increasing the delay by more than 4 μsec after the first STOP may result in a degradation in module performance.

Clear : Resets the Hit Register and the front ends as follows:

100, 200, 400, 800 nSec Full Scale:
t < (COMMON - 850 nSec): resets any channels that have received START signals; no effect on digitization.
(COMMON - 700 nsec) < t < DIGITIZATION: resets front ends and aborts digitization cycle.
t > DIGITIZATION: resets front ends; no effect on digitization.

1, 2, 4, 8 μSec Full Scale:
t < (COMMON - 2.2 μsec): resets any channels that have received START signals; no effect on digitization.
(COMMON - 1.9 μsec) < t < DIGITIZATION: resets front ends and aborts digitization cycle.
t > DIGITIZATION: resets front ends; no effect on digitization.

BUSY is asserted following clear to allow time for the front ends to fully reset.

Inhibit : Inhibits TAC and digitization. Must be removed at least 10 nSec before START or COMMON signals for those signals to be recognized.

Front End Inhibit: must be applied no later than the START signal.

Digitization Inhibit: must be present 10 nSec before the COMMON .lh8 input to inhibit digitization.

Test Function: Common to all channels. Used in conjunction with the COMMON START/STOP input to test operation of the TDC anywhere within the range.

BUSY OUTPUT

7186 : Lemo output. NIM current switching bridged output (32 mA).

7186H : ECL output. Two differential pairs.

Active as follows:

From receipt of COMMON until the event has been aborted by a Fast Clear or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register.

For 800 nSec following FAST CLEAR (2.4 μSec for ranges $\geq$ 1 μSec).

During any CAMAC addressing of the module.

FRONT END PERFORMANCE

START/STOP Pedestal : 20 nSec. Front ends are offset this amount to allow use of full dynamic range.

Linearity : Integral - < 3 counts over 10% to 90% of range.
Differential - <.025% of full scale.

FRONT END PERFORMANCE (continued)

Noise, Jitter	:	Typically < 20 pSec RMS.
Crosstalk	:	< 3 LSB maximum between adjacent channels.
Stability	:	Gain: 100 ppm/°C typically. Offset: .15 counts/°C typ.

POWER REQUIREMENTS:

+6V - 2.7 Amps typically
- 6V - 2.2 Amps typically
+24V - 180 mA typically.
Forced cooling is recommended.

ADDITIONAL TEST FEATURES

Calibration Check	:	Simulates a Start/Stop sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration for each full scale range. Not intended for use in calibrating the module.
CAMAC Check	:	Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the digital processing sections of the module.

SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset; when the final channel has been read LAM is reset. LAM is also reset when the Hit Register is reset.

DATA WORD FORMAT

16 13	12 1
Channel ID	Channel Data

CONTROL REGISTER FORMAT

16 9	8 4	3	2	1
Conversion Delay (Read Only)	0	UT Enable	LT Enable	PED Enable

CAMAC DATAWAY OPERATIONS

F(0)·A(X)	:	Read event data memory for Channel (X+1). Data word as described above.
F(1)·A(X)	:	Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).
F(4)·A(0)	:	Read Sparse Data. Only those channels with data that falls between the upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.
F(6)·A(0)	:	Read the Control Register. Format described above.
F(6)·A(1)	:	Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.
F(8)	:	Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

CAMAC DATAWAY OPERATIONS (Continued)

F(9)	:	Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.
F(10)	:	Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.
F(11)·A(0)	:	Reset the Control Register. Occurs on S2 strobe.
F(11)·A(1)	:	Reset the hit register and LAM. No effect on data memory. Occurs on S2 strobe.
F(11)·A(2)	:	Reset the test register. Occurs on S2 strobe.
F(11)·A(3)	:	Reset the hit register, LAM and data memory. Occurs on S2 strobe.
F(16)·A(X)	:	Write to data memory for channel (X+1).
F(17)·A(0)	:	Select the Pedestal Memory for the next F1 or F20 operation.
F(17)·A(1)	:	Select the Lower Threshold Memory for the next F1 or F20 operation.
F(17)·A(2)	:	Select the Upper Threshold Memory for the next F1 or F20 operation.
F(17)·A(4)	:	Select the Test Register for the next F20 operation.
F(19)·A(0)	:	Set the Control Register bits. Format described above.
F(20)·A(X)	:	Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095; threshold ranges are 0 - 4095. Program the test register if it was selected by the most recent F17 operation. A0 : Test pattern = 001001001001 A1 : Test pattern = 010010010010 A2 : Test pattern = 100100100100 A3 : Test pattern = 111111111111
F(23)·A(0)	:	Reset the Control Register bits. Format described above.
F(24)	:	Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.
F(25)·A0	:	Digital test. Initiates a data acquisition cycle using the value stored in the test register by the most recent F20 command.
F(25)·A1	:	Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.
F(25)·A2	:	Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.
F(26)	:	Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

CAMAC NON-DATAWAY COMMANDS

C, Z	:	Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the hit register. Occurs on the S2 strobe.
I	:	Inhibits TDC Front End.

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