Model 4504
Flash ADC

Inputs: Four on coaxial connectors, 50 Ω ±5% impedance, 10 nsec minimum width. Analog input range user defined between -2.5 V and +2.5 V. Range, set by computer command by giving low and high voltage reference levels, is divided by 15 to obtain resolution (4 bits).
Strobe: One ECL input for external strobe selected by front-panel switch. Leading edge initiates digitizing of all four inputs simultaneously; falling edge transfers digitized values to outputs and holds until next strobe. Maximum frequency 100 MHz. Alternate switch setting provides internal 20 MHz – 100 MHz free-running strobe. Internal strobe frequency set by front-panel adjustment.
Veto: One ECL input inhibits strobe signal.
Outputs: Four, 4-bit ECL outputs on 8-pin headers. Overflow bits provided on 4 two-pin headers.
Strobe Out: Two on two-pin headers (ECL pulses) and two on Lemo connectors (-600 mV pulses) timed with digital outputs for downstream logic. Width is adjustable by front-panel potentiometer in the range of 5 to 25 nsec.
Test Points: Two front-panel test points permit measurement of voltage reference levels.
Input-Output Delay: Strobe trailing edge to digital outputs, typically 15 nsec.
Power: 1.1 A at +6 V; 1.5 A at -6 V; 6 mA at +24 V (15.7 W total).

Model 4508
Programmable Lookup Unit

Inputs: Two, 8-bit inputs on 34-pin header, 110 Ω ±5% for complementary ECL. Minimum width 10 nsec, maximum rate 65 MHz.
Strobe: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires -600 mV signal, 5 nsec minimum width and must precede input by 2 nsec for exact time coincidence. Latches inputs, except in overlap mode. Maximum frequency > 65 MHz. Strobe must be followed by clear except in Overlap Mode.
Clear: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires -600 mV signal, 5 nsec minimum width to clear. Clears pattern register and resets outputs in all modes.
Outputs: Two, 8-bit outputs on 34-pin headers, ECL signals. Width of output in Shaped mode set by front-panel adjustment between < 5 nsec to > 100 nsec.
Synchro Output: Two on Lemo connectors, one per output section, 50 Ω impedance. Supplies -600 mV pulse out when outputs are ready. Typically used for strobing next unit, or for self-clearing.
Modes: Overlap (OVL) - Output pulse width determined by coincidence between Inputs and Strobe. Shaped (SHP) - Output pulse width is determined by a front -panel adjustment from < 5 to > 100 nsec. The unit must be cleared before another input can be latched. Continuous (CNT) - Output state is latched by the Strobe, until a Clear is applied.
Propagation Delay: (17 ±3) nsec in Overlap Mode. In other modes (21 ±1) nsec independent of logic function and determined by Strobe timing.
Power: 0.5 A at +6 V; 2.6 A at -6 V (18.6 W total).

Model 4516
Programmable Logic Unit

Inputs: 16 sets of three inputs, 110 Ω ±5% (high impedance by removal of socketed terminators), DC-coupled, on 34-pin headers, for ECL signals, minimum 2 nsec rise time. Maximum rate 150 MHz.
Veto: One rear-panel Lemo connector, 50 Ω impedance. Requires -600 mV signal. Permits gating of outputs, including OR outputs. Must overlap coincidence for the three front-panel inputs by > 5 nsec.
Outputs: 16, one per set of three inputs, complementary ECL logic levels on 34-pin header.
OR Out: Two, one for OR of first 8 outputs, one for second 8 outputs (factory option permits OR'ing of all 16 outputs).
Double Pulse Resolution: 5 nsec at minimum input width.
Coincidence Width: > 3.5 nsec determined by input pulse width.
Input-Output Delay: A or B to OUT by 11 nsec typical; A or B to OR by 12 nsec, typical; C to OUT by 8 nsec, typical; C to OR by 9 nsec, typical; VETO to OUT by 8 nsec, typical; VETO to OR by 6 nsec, typical.
Power: 50 mA at +6 V; 1.25 A at -6 V (7.8 W total).

Model 4518 (formerly 4418)
Programmable Logic Delay/Fan-Out

Inputs: 16, DC coupled 110 Ω ±5% impedance, on 34-pin header for ECL signals; 100 MHz maximum rate (> 35 MHz for 4518/300), < 10 nsec double pulse resolution (< 30 nsec for 4518/300). Minimum width: 5 nsec, (15 nsec for 4518/300).
Delay: 1-16 nsec in 1 nsec steps (4518), 2-32 nsec in 2 nsec steps (4518/100), 8-128 nsec in 8 nsec steps (4518/300). Delays set by computer for each channel individually.
Outputs: Three for each input, on three 34-pin headers, for compatibility with complementary ECL devices. Width equal to input duration ±1.2 nsec (±4 nsec 4518/300). Rise time and fall time: 2.5 nsec.
Crosstalk: Synchronous pulses in adjacent channels can be affected by ±1 nsec typical.
Power: 50 mA at +6 V; 2.5 A at -6 V (15.3 W total).

Model 4532
Majority Logic Unit

Input: All inputs accept differential ECL level (-0.8 V, -1.7 V) into 110 Ω ±5% input impedance (high input impedance is possible by removing socket-mounted terminators).

Output: All logic outputs provide complementary ECL levels (-0.8 V, -1.7 V) and are capable of driving differential 110 Ω loads.
Data Input (IN): 32 in two 34-pin front-panel connectors; minimum input pulse width 6 nsec.
Reset Input (RTI): Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI resets only the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec. In Memory Disable mode, the RTI is inhibited.
Gate Input (GAI): Normally open when unconnected. Normally closed when connected to a cable providing standard ECLine levels. In Memory Disable Mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable Mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical ORs, 3 nsec.
Cluster Carry (CCI): When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Carry Output (CCO) of any adjacent majority logic unit.
Analog Majority Input/Output (AMIO): High impedance current source; AMIO connectors can be used for daisy chaining of analog majority information within a unit. Generates current proportional to the input multiplicity at the rate of 3.2 mA per unit. Generates current proportional to the unit multiplicity at the rate of 3.2 mA per hit. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 Ω.
Data Outputs (OUT): 16 in a 34-pin front-panel connector. In Memory Disable Mode, provides pulses corresponding to an overlap coincidence between the gate pulse & the data inputs. In Memory Enable Mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.
OR Output (ORO): Provides the logical OR of the 32 channels, otherwise behaves as data outputs.
Strobe Output (STO): Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.
Majority Discriminated Output (MDO): The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front-panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.
Delayed Majority Output (DMO): Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges; 10-100 nsec or 50-1000 nsec. A front-panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.

Cluster Carry (CCO): When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI) input.
Mode Selection: A Memory Enable switch, accessible on the side of the module, selects one of the following modes: Memory Disable - Functions are disabled; the multiplicity calculation is performed on the overlap of the data inputs. Memory Enable - The data inputs are latched; the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a CAMAC reset function.
Cluster Selection: The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes: Cluster Disable - Each data input provides one hit on the Analog Majority Output AMIO; the Cluster Carry Input (CCI) is disabled; Cluster Enable - Any group of adjacent input data pulses will be considered as a single hit. Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.
Input-Output Delay: Data IN to AMIO - 16 nsec; AMIO to MDO output -5 nsec; End of gate IN to Strobe OUT by 6 nsec; Data IN to Data OUT by 12 nsec; Data IN to OR OUT by 16 nsec; Reset IN to Data OUT by 20 nsec; Reset IN to OR OUT by 24 nsec; Data IN 32 to Cluster Carry OUT by 11 nsec; Cluster Carry IN to Data IN 1 by 2 nsec. Gate pulse must precede Data pulse by at least 7 nsec.
Power: 200 mA at +6 V; < 3.6 A at -6 V; 5 mA at +24 V; 7 mA at -24 V (23 W total).

Model 4564
OR Logic Unit

Inputs: 64 in four 34-pin front-panel connectors, ECL signals, 110 Ω impedance. Minimum width 6 nsec, maximum frequency > 100 MHz.
Overlap Outputs: Rear-panel 34- pin connector, pins 1 to 12, ECL signals. Width corresponds to overlap (±2 nsec) of inputs of logic function, minimum output 5 nsec, maximum output frequency > 100 MHz; transit time 12 nsec ±1 nsec typical, independent of logic function; double pulse resolution 10 nsec typical.
Shaped Outputs: Rear-panel connector pins 13 to 16, any of overlap logic can be converted via jumper option to any of the four discriminator/shapers, output is differential ECL levels and width is internally adjustable from 15 to > 500 nsec, can be triggered in leading or trailing edge of inputs (jumper selectable); output polarity internally switch selectable; maximum frequency: 30 MHz, double pulse resolution: 33 nsec.
Power: 150 mA at +6 V; 1.5 A at -6 V; 20 mA at -24 V (10.4 W total).