Product Description

2.1 Introduction

The LeCroy Model 1876 provides 96 channels of either common start or common stop multihit Time to Digital Conversion designed for elementary particle or nuclear physics experiments. All input time signals to be measured ('hits') are received via differential ECL (dECL) front panel inputs. Each channel exhibits 1.0 nsec LSB and can store up to 16 hits within a 65.536 μsec range. The time measurement is performed using the MTD132A, a full custom ASIC developed by LeCroy Corporation.

2.2 General Description

The 1876 Time to Digital Converters offers all the flexibility of the 1870 Series Pipeline Time to Digital Converters with a 1 nsec least count and can store up to 16 hits per channel within a 65.536 μsec full scale range. Lower and upper time discriminators can be programmed, allowing the user to select the time window of interest.

Each 1876 has 96 channels of front panel inputs and a common input. All inputs are differential ECL (dECL) and are terminated by a balanced 110 ohm impedance matching network. The 1876 can operate in either common start or common stop mode. In common start mode, the common input receives a start pulse and the individual channels can register up to 16 stops. In common stop mode, the 96 front panel inputs register individual channel hits and the common inputs latches a stop pulse. Each channel can be programmed to detect leading and/or trailing edges (hits) and can store up to 16 hits. Selected edges can be detected with as little as 20 nsec separating them (see Section 4.2). If more than 16 hits occur per channel, only the last 16 hits are retained. Multiple common input pulses are prohibited, only the first is registered.

Operation of the 1876 can be thought of in four phases: programming, acquisition, buffering and readout. Once the control and status registers have been programmed the module is in acquisition mode and ready to latch hits. In common start mode, the acquisition phase begins when the module latches a start and ends after a user programmable time period. No hits will be recorded after the programmed hit window expires. A front panel dECL input is provided to allow the use of an external time out if desired. However, the maximum acquisition time is internally set to 65.536 μsec. Immediately following the acquisition phase, the data is placed in a eight event buffer awaiting readout. (Buffer structure differs for Mod 100, See Section 6). Readout can occur as quickly as 1 usec after the end of acquisition. The module automatically returns to acquisition mode once all the data has been safely buffered.

A programmable fast clear window begins immediately following the end of acquisition. During the fast clear window (FCW), a user can safely clear an event based on a trigger decision and return to acquisition mode, thus saving the time necessary for buffering and reading out the event. The FCW can range from 800 nsec to 400 usec, depending on the needs of the user.

The data for each event is preceded by a header word identifying the address (geographic or logical), the buffer number, and the word count for the event. A parity bit is set to give an even number of bits for the word. The timing measurements of the 1876 are stored as 32 bit words. The 16 least significant bits are the time measurement; the next 7 bits contain the channel information; the next bit is the phase bit denoting the slope of the edge; the next seven bits are the channel identification;the next two bits are modulo 2 the buffer address; the next bit is the parity bit (even); and the 5 most significant bits contain the geographical address of the module.

Trigger signals are pairwise OR'ed for each pair of signals (0&1, 2&3, etc.) These can be programmed to generate a single pulse or multiple pulses of specified length during the event. If selected for single pulse operation, only one trigger pulse, of the programmed duration, will be output for a channel pair regardless of how many hits arrive on that channel pair during the event. If multiple pulse operation is enabled, a trigger pulse will be output for every hit on the channel pair. If both

leading and trailing edge detection are selected, a trigger pulse will occur for each edge. These signals are prompt and are provided at the auxiliary connector. There is a small amount of jitter on the trigger pulses at the auxiliary connector with respect to the front panel input. This jitter is +/− 16 nsec for the 112 nsec trigger pulse width and 8% of the trigger pulse width for all other trigger pulse widths.

The functionality of the 1876 can be tested using either an internal tester or a front panel dECL test input. The internal test can be programmed to produce 1, 2, 4 or 8 pulses separated by 96, 192, 768 or 1536 nsec. Either or both edges of the pulses are selectable for detection, creating up to 16 internal hit per channel. Internal tester hits may be applied to the odd and/or even channels simultaneously. Testing can be performed in both common start and common stop modes.

Like the earlier LeCroy model 1878 & 1879 model TDCs, provisions have been made to accomodate auxiliary card functions. A 12 bit bi−directional bus, four address lines and three control lines have been connected to the Fastbus auxiliary connector for read and write operations on the auxiliary card. All 48 trigger outputs have also been connected for fast triggering. The 1876 also has the facility to allow auxiliary cards to assert the TDC's T−pin in response to a given broadcast code. Pinout at the auxiliary connector is compatible with the earlier models.

2.3 Specifications

Please refer to the model 1876 technical data sheet for a complete summary of all relevant specifications.

2.4 Front Panel

The LeCroy Module 1876 TDC front panel provides the user with connectors for system integration and LEDs to assist system debugging. Cables necessary for proper installation can be purchased from LeCroy. See Section 3.2 for more information regarding cabling.

2.4.1 Displays

Two colored LEDs exist on the front panel of the 1876 to indicate the status of operations. A brief description of each is listed below: The LED illumination is stretched to a minimum of 10 msec to aid in viewing.

- **Slave Addressed LED:** As per the Fastbus specification, this yellow LED is lit whenever the TDC module is attached to the Fastbus as a slave.

- **Com Hit LED:** This green LED is illuminated whenever the TDC registers a common hit (start or stop). The common hit may come via the front panel input marked COM or it may be created by the module on-board tester. See Section 2.8 for more information regarding the on-board tester.

2.4.2 Inputs

All front-panel inputs to the 1876 are differential ECL compatible with the ECLine standard. All inputs are differentially received. The "+" input is quiescently at least 200 mV more negative than the "-" input. Each pair of differential inputs is terminated with an effective 112 ohms.

All hit inputs are received via six 34 pin connectors. A 3M connector type 3414-6034 will mate with the TDC header and provide strain relief. Pin 33 is connectde to circuit ground, and pin 34 is connected to chassis ground. The circuit ground and the chassis ground are connected to each other on the printed circuit board through 100 ohms. The hit inputs are numbered from top to bottom in ascending order. Four control inputs are differentially received via an 8 pin header located at the bottom of the front panel.

The control signals can be connected by single pair headers AMP part number 5-87456-2 or they can all be connected simultaneously by a 8 position connector AMP part number 87456-2. A brief description of each input follows below:

- **COM:** A dECL input which receives the common input pulse. Any pulse, whether it be a start or a stop, received via the COM input is global to all 96 channels. In common start mode the pulse acts as a global start for every channel, and in common stop mode it acts as a global stop for every channel. Front panel input of this signal is selected by setting CSR1<1> to 0. This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module in the chain.

- **CLR:** A dECL input used to issue fast clears to the module. A clear pulse can be issued at anytime inside the Fast Clear Window or when buffering is not in progress, provided it is at least 40 nsec wide. When a clear is issued, the data of a just measured, unbuffered, event is cleared and the module returns to acquisition mode 150 nsec after the trailing edge of the pulse. There is no output signal coinciding with the module's return to the ready state. The control and status registers are not affected by a clear. Front panel sourcing of this signal is always enabled. This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module in the chain.

- **TIME:** A dECL input used to receive the common start timeout pulse. When operating in common start mode, it is necessary to define a period of time when the TDC will register hits. The beginning of this period starts with receipt of the Common Start. The end of this time occurs when the module receives the timeout pulse. Front panel input of this signal is selected by setting CSR1<7:4> to 0. This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module

in the chain. This signal can also be provided by an on board programmable timer. If the front panel source for this signal is selected but does not arrive, the module will still time out after 65 usec.

- **IN:** All 96 dECL inputs are used to receive individual channel hits. In common start mode the stop pulses are received via the connectors marked IN, and in common stop mode the start pulses are received.

2.4.3 Outputs

The one front panel outputs from the 1876 is differential ECL The "+" output should be quiescently at least 200 mV more negative than the "−" output. This output is terminated with 112 ohms to −2 V.

- **BIP:** Buffering in Progress (BIP) is a single dECL signal provided to aid in readout. While BIP is true, the current event's data is being buffered and the data from this event is not ready for readout via FASTBUS. BIP will also become true when all buffers care full and no further events can be accepted. In the event of a fast clear, BIP will go false within 75 nsec. of the rising edge of the fast clear pulse. See Section 6 for Mod 100 variations.

2.5 Control and Status Registers

Twenty three Control and Status Register (CSR) locations are possible. Seven registers reside on the 1876 TDC module itself and are always implemented within the module. Sixteen additional locations are reserved for an Auxiliary Functions Card (AFC) are are supported by the Fastbus interface to the auxiliary connector. These 16 registers exist only to the extent they are implemented on the AFC.

2.5.1 Control and Status Register 0

When CSR 0 is read, the 1876 presents $103B_h$ on the Address/Data bus lines 16–31 as its manufacturer's identification (see Section 6 for Mod 100 manufacturer's identification). CSR0 is the default register when a primary address to control space is issued. See Figure 2–1 and Figure 2–2 for individual bit definitions.

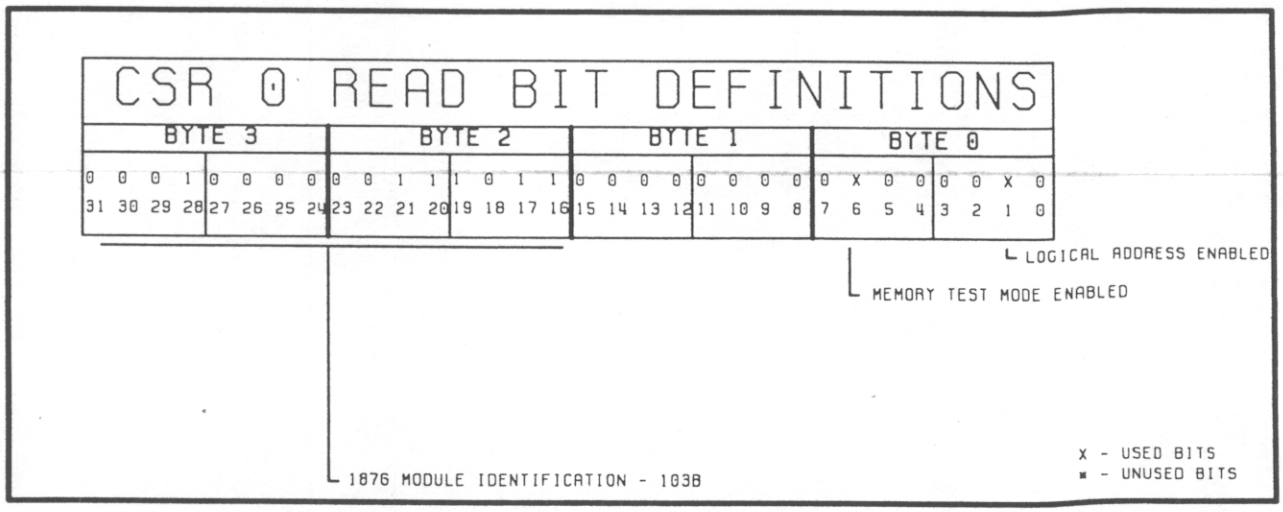

Figure 2–1 CSR0 Read Bit Definitions

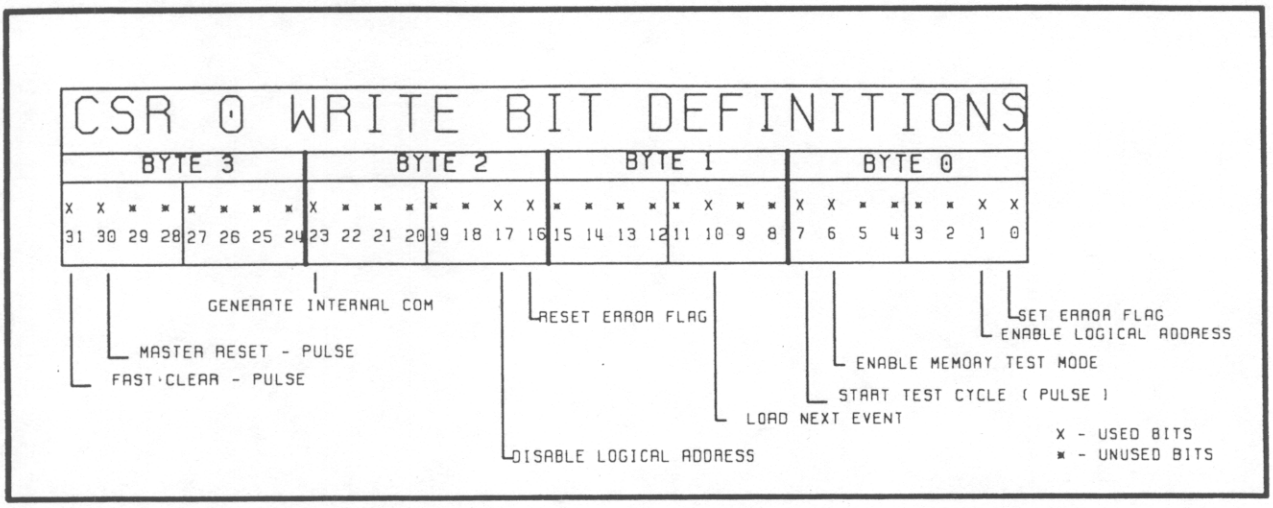

Figure 2–2 CSR 0 Write Bit Definitions

CSR 0 after Master Reset or power–up: 103B 0000

Latched Bits:

- **Logical Address Enable:** Bit 1 must be set for the unit to respond to logical addressing.
- **Memory Test Mode Enable** : If Bit 6 is set, the memory in data space may be accessed by specifying an NTA in data space corresponding to the memory location desired. This feature may be used to facilitate testing of the memory. In normal operation, this bit should be 0.

Pulsed Bits:

- **Fast Clear:** Writing Bit 31 will produce a clear signal equivalent to a front panel clear or TR0 clear.
- **Master Reset:** A write to Bit 30 will reset all CSR's to their power up condition.
- **Load Next Event:** This input advances the read pointer of the buffer by 1 and loads CSR5 with the word count for that event. This facilitates a block read of the event. Not supported in Mod 100, see Section 6.
- **Test Cycle:** A write to Bit 7 initiates a burst of pulses from the internal tester.
- **Internal Com:** Writing Bit 6 is equivalent to a pulse on the front panel Com (or TR6 input). This method of generating a Com signal is always enabled.
- **Set Error Flag:** No operating condition on the 1876 generates an error flag at this time. This is included for possible future use. This bit can be set by writing CSR0<0> and reset by writing CSR0<16>.

2.5.2 Control and Status Register 1

The information necessary to define such user–programmable functions as the acquisition mode, the edge detection, the fast clear window, the internal tester's operation and the trigger mode are contained within CSR 1. See Figure 2–3 for individual bit definitions.

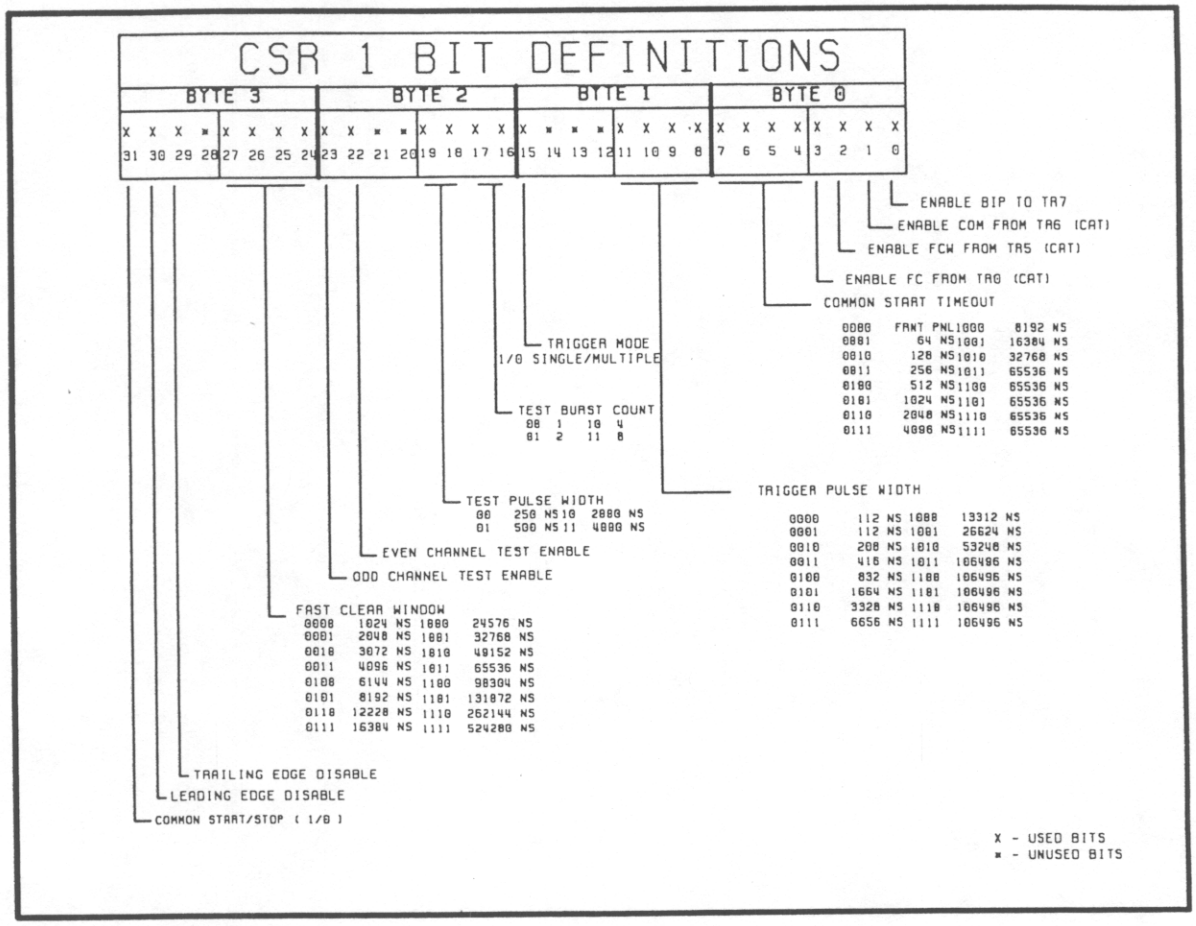

Figure 2–3 CSR1 Bit Definitions

CSR1 after Master Reset or power–up: 0000 0000

- **Acquisition Mode:** Bit 31 determines whether the TDC will operate in common start or common stop mode. When a one is written the board operates in common start mode, and when a zero is written the board operates in common stop mode. When read, the status of the bit is presented.

- **Leading Edge Enable**: Bit 30 determines whether the TDC will register the rising (low–to–high transisitions) edges of incoming hits. Hits may be received from either the front panel IN connectors or the on–board tester. When a one is written the board will not detect rising edges, and when a zero is written the board will detect rising edges. When read, the status of the bit is presented.

- **Trailing Edge Enable:** Bit 29 determines whether the TDC will register the trailing (high–to–low transisitions) edges of incoming hits. Hits may be received from either the front panel IN connectors or the on–board tester. When a one is written the board will not detect trailing edges, and when a zero is written the board will detect trailing edges. When read, the status of the bit is presented. See Sec. 6 for Mod 100 differences.

- **Fast Clear Window:** Bits 24–27 determine the length of time the on–board timer permits the user to issue a fast clear to the module after the end of acquisition. The fast clear window begins immediately following a stop pulse in common stop mode and immediately following a

common start timeout in common start mode. Note, this is independent of a Fast Clear Window supplied from the 1810 CAT module; the two sources are in effect OR'ed together. Once the fast clear window has ended, the current event can no longer be cleared from the multi-event buffer. When read, the status of the bits is presented.

- **Odd Channel Test Input:** Bit 23 determines whether the odd channels of the 1876 will receive the test inputs. When read, the status of the bit is presented.

- **Even Channel Test Input:** Bit 22 determines whether the even channels of the 1876 will receive the test inputs. When read, the status of the bit is presented.

- **Test Pulse Width:** Bits 18 and 19 determine the width of the on-board tester's hit pulses. The width can be programmed to be 250, 500, 2000 , or 4000 nsec when a 0, 1, 2 or 3 are written respectively. When read, the status of the bits is presented.

- **Tester Burst Count:** Bits 16 and 17 determine the number of pulses the on-board tester will generate. The tester can be programmed to create 1, 2, 4 or 8 pulses when a 0, 1, 2 or 3 are written respectively. When read, the status of the bits is presented.

- **Trigger Mode:** Bit 15 determines whether the 1876 will present a single or multiple trigger pulses on the auxiliary connector as result of hits. When a one is written, the 1876 will latch the hit for a given channel pair; the corresponding signal coming out of the auxiliary connector will be only one pulse of the programmed duration until the end of the event. When a zero is written, the 1876 will present a programmable width pulse on the auxiliary connector for every hit the TDC detects. When read, the status of the bit is presented.

- **Trigger Pulse Width:** Bit 8-11 determine the width of the trigger pulse presented on the auxiliary connector when the TDC is operated using a pulsed trigger mode. The pulse can be as narrow as 112 nsec and as wide as 106,496 nsec. When read, the status of the bits is presented.

- **Common Start Timeout:** Bits 4-7 determine the measurement full scale in common start mode. These bits define the period of time during which the TDC will detect hits. It is initiated by a start pulse and ended a variable time later by the timeout. The timeout can be programmed to arrive as quickly as 64 nsec after the start pulse or as long as 65,536 nsec after the start pulse. The common start timeout is only meaningful in common start mode. When read, the status of the bits is presented.

- **Enable Fast Clear from TR0:** Setting Bit 3 to 1 permits receipt of a fast clear from TR0. The front panel source of fast clear remains enabled.

- **Enable FCW from TR5:** Setting Bit 2 to 1 permits a fast clear window to be supplied from TR5.

- **Enable COM from TR6/TR3:** If Bit 1 is set to 1, either TR6 or TR3 is enabled as the source for the COM signal, and the front panel COM is disabled. If the 1876 is in Common Stop mode, the TR6 is the source. If in Common Start mode, TR3 is the source. See Sec. 2.9 Writing CSR0<6> is always enabled.

- **Enable BIP to TR7:** Setting Bit 0 to a 1 outputs the Buffering in Progress signal to TR7. This should not be set if a model 1810 CAT is in the same crate.

2.5.3 Control and Status Register 3

As per Fastbus specification, CSR 3 contains is used to store the desired logical address for the unit. CSR3<31:16> contain the logical address. This register powers up to 0 but is not disturbed by a master reset, CSR0<30>.

2.5.4 Control and Status Register 5

CSR 5 is implemented as an 11 bit read/write register used to give an indication of the number of words transferred. During a FASTBUS readout, it is decremented after each transfer. The word count is automatically loaded for the next event to be read out after a load next event has been issued. Bits 0 through 10 only are meaningful. Bits <15:11> will read back as 0. Bits <31:16> are not defined for read. CSR5 is set to 0000 0000 by a Master Reset. See Section 6 for mod 100 variations.

2.5.5 Control and Status Register 7

CSR 7 is used to specify the broadcast classes to which an 1876 will respond. It is implemented as an 8 bit read/write register. Bits 7 through 0 correspond to broadcast classes 7 through 0 respectively. If bit N is set, the 1876 will be selected by a broadcast to class N devices. CSR7 is not affected by Master Reset.

2.5.6 Control and Status Register 8

Not implemented for Revision A.

2.5.7 Control and Status Register 16

CSR 16 is implemented as a 16 bit read-only register used to indicate the location of the read and the write buffer addresses. CSR 16 <15:8> indicate the next buffer to be readout, and CSR 16 <7:0> indicate the next buffer address to be filled. CSR 16 <10:8> are the same as the Data Space NTA <13:11>. The read buffer pointer is modifed by any modification of the Data Space NTA and the write buffer pointer is only modified by 'Load Next Event' feature and master reaset. Master Reset and Power-up reset CSR16 to 0007 0000.

This register is not supported in Mod 100, see Section 6.

2.5.8 Control and Status Register 17

Not implemented for Revision A.

2.5.9 Control and Status Register 18

CSR 18 can be programmed to act as a time discriminator. Both a lower and an upper limit can be set. Only time measurements falling between the lower and upper limits will be stored in the multi-event buffer; other data will be discarded. Both limits can range from 0 nsec to 65,536 nsec and can be varied in steps of 16 nsec.

This register resets to all zeroes, which will not pass any data. CSR18 must be programmed to cause a non-zero time window after Power-up or a Master Reset.

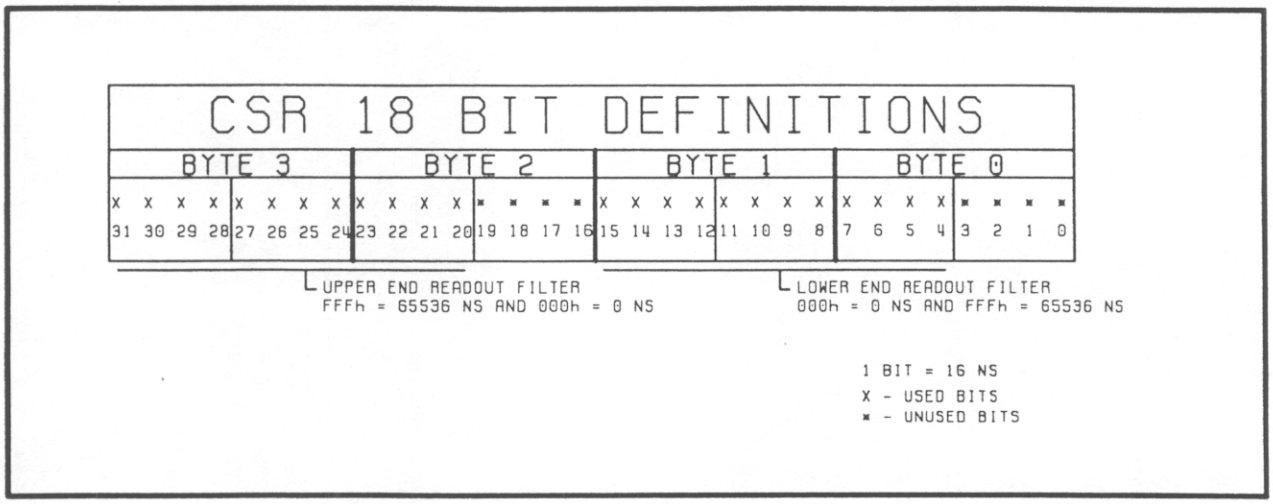

Figure 2–4 CSR18 Bit Bit Definitions

- High End Discriminator: Bits 20–31 can be programmed to define an upper end time discriminator. Only time measurements (start to stop) less than upper limit will stored in the multi–event buffer.Please note that since this is a greater than comparison and the least 4 bits of the 16 bit time measurement are ignored, writing 0x000 to bits 20–31 will still pass data which is less than 16 nsec. Writing a 0x001 will pass data up to 31 nsec in magnitude. When read, the status of the bits is presented.

- Low End Discriminator: Bits 4–15 can be programmed to define a lower end time discriminator. Only time measurements (start to stop) greater than the lower limit will be stored in the multi–event buffer.Writing a 0x000 to bits 4–15 will pass all data. Writing a 0x001 to bits 4–15 will reject data less than 16 nsec in magnitude. When read, the status of the bits is presented.

- Unused: Bits 0–3 and bits 16–19 are not used. However, the bits are physically available, thus they may be programmed to any status. When read, the status of the bits is presented.

2.6 FASTBUS Operations

2.6.1 FASTBUS Address Cycles

The 1876 TDC responds to geographical, logical and broadcast addressing.

2.6.1.1 Logical Addressing

CSR3<31:16> contain the logical address to which the 1876 will respond in both CSR space and Data space.

2.6.1.2 Geographical Addressing

The model 1876 responds to geographical addressing in both CSR space and data space.

2.6.1.3 Broadcast Addressing

The following is a list of Broadcast operations responded to by the 1876. The case numbers are from the IEEE 960–1989 Fastbus specificaton, Table 4.3.2. Example address use G=0 and L=1 for broadcasts on the local FASTBUS segment only.

- **Case 1:** General Broadcast. 0x00000001. All devices respond to subsequent data cycles.
- **Case 2:** 0x00000005. Only devices of class N respond to subsequent data cycles.
- **Case 3:** Sparse Data Scan: Devices respond by asserting T-Pin during following read cycle if data present. e.g. 0x00000009.
- **Case 3a:** Sparse Data Scan: 0x00000019. Devices respond by asserting T-Pin if they contain no data or are available for use.
- **Case 4:** 0x0000000D. Devices respond by asserting T-Pin during following read cycle.
- **Case 8-B:** 0x000000BD. Devices respond by asserting T-Pin during following read cycle if the auxiliary card is asserting PCT.
- **Case 8-C:** 0x000000CD. Unique 1876 Sparse Data Scan: 1876 TDCs respond by asserting T-Pin during following read cycle if unsuppressed data is present in the next buffer.

CSR7<7:0> controls the classes of class N broadcast to which the 1876 will respond in both Data and CSR spaces.

2.7 Data Space

Data resulting from an event is stored in one of eight 2048 word buffers (Buffer structure for 1876 Mod 100 differs, see Section 6 for discussion). Each event buffer contains enough addresses to hold the maximum data resulting from a single event (1537 words). An event is defined as the occurance of a Common Start or Stop. In normal acquisition Memory Test Mode is disabled, and the 1876 data space consists only of DSR0; any NTA write has no effect.

The data storage area acts as a circular buffer for normal data acquisition. CSR16 shows the status of the buffer pointers (Read pointer and Write pointer). CSR 16 <2:0> specify the next event buffer to be filled and CSR16<10:8> specify the next event buffer to be read. When a master reset is issued or at power-up, the next event buffer to be read will be 7, and the next event buffer to be filled will be 0. Before readout of the first event can occur, a Load Next Event command must be issued (CSR 0 <10>) to move the read buffer pointer to 0. Once an event occurs and is buffered the write buffer pointer is automatically incremented. CSR16 can not be written from Fastbus. CSR16<10:8> can only be changed by doing a Load Next Event (writing CSR0<10>).

CSR 5 <10:0> controls the number of words transferred in a block read. During normal data acquisition, a Load Next Event both advances the buffer read pointer to the next event and loads CSR 5 <10:0> with the correct word count for the event. This can of course be done for an entire crate at once using a broadcast command.

When the read pointer is one less than the write pointer (modulo 8) the buffers are considered empty. When the read pointer and the write pointer are equal, the buffers are considered full. The condition 'not empty' is used for the Sparse Data Scan. The condition 'full' is used to extend Buffering in Progress (BIP) until the buffers are not full.

When Memory Test Mode is enabled(CSR0<6> = 1), any address within the 16K memory area may be randomly read or written via standard FASTBUS data cycles. The NTA specifies the memory location of interest.

2.7.1 Header Word Format

The zeroeth address of each page contains a header word for the event data which follows . This header word contains the word count for that event. The word count is automatically loaded into CSR 5 when a Load Next Event command is issued. After each FASTBUS data cycle, the word count register is decremented. The parity bit is high or low so as to make the total number of bits in the

header word even.

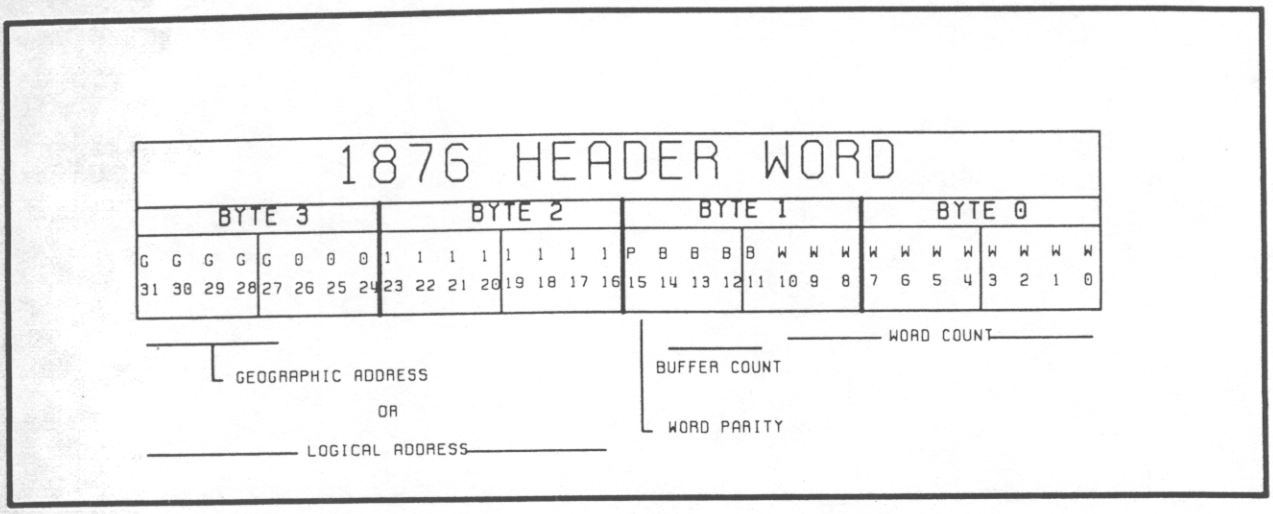

Figure 2–5 1876 Header Word

2.7.2 Data Format

The 1876 data is read out as a 22 bit data word. The 16 least significant bits are the data, the next bit is the hit phase (denoting leading or trailing edge), and the next 5 bits are the channel identification. The hit phase is one for a leading edge hit and zero for a trailing edge hit. Here again the parity bit is high or low so as to make the total number of bits in the word even.

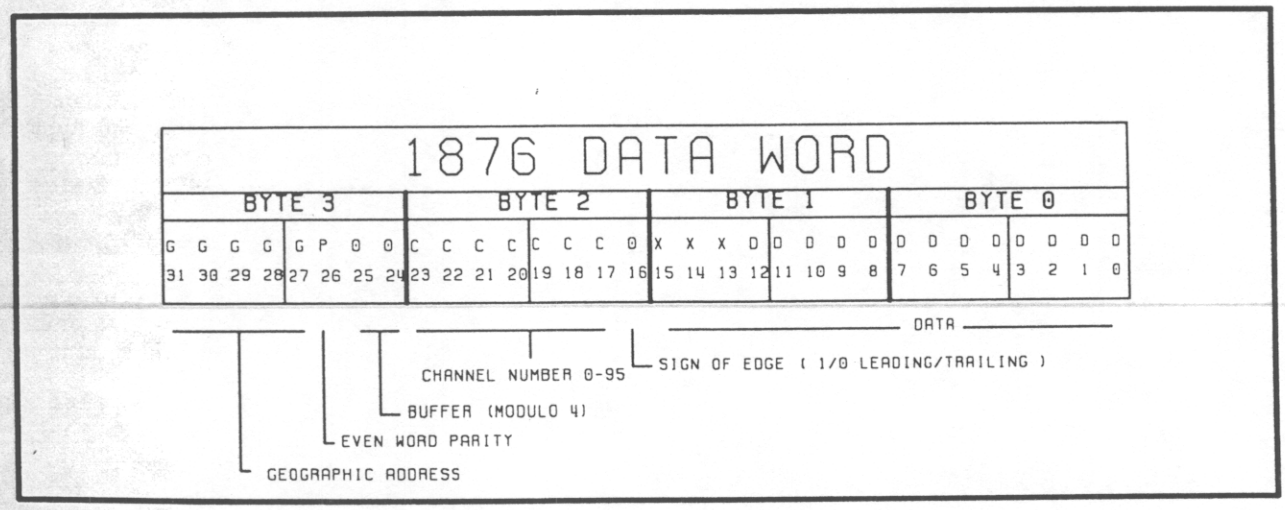

Figure 2–6 1876 Data Word

2.8 Tester

An on board tester is provided for easy verification of the unit's functionality. When CSR0<7> is written, a test cycle of square wave pulses is initiated. The number of pulses generated can be 1, 2, 4, or 8 as programmed by CSR1<17:16>. The width of the pulses is controlled by CSR1<19:18>. By enabling both leading and trailing edge sensitivity (CSR1<30:29> = 0), setting the tester to 8 pulses, and enabling both even and odd channeltesting (CSR1<23:22> = 3), it is possible to generate 16 measurements on 96 channels.

read and write operations on the auxiliary functions card (AFC). The three control lines are sufficient to control the data flow to or from the AFC. Two of the three control signals are originated by the Fastbus master: the Auxiliary Read (AUXR) signal and the Auxiliary Clock (AUXC) signal. The AR is simply the Fastbus Read (RD) signal AND'ed with the Auxiliary Select signal (AUXS). The AUXC signal is simply the Fastbus Data Stobe (DS) signal AND'ed with the AUXS signal. The AFC is accessed when a secondary address to control space with an address of C000000Xh is performed.

The Auxiliary Functions connector also has the facility to allow the AFC to assert the TDC's T-pin in response to a BDh broadcast read. The AFC need only drive the PCT line low to assert the T-pin.